American Journal of Engineering Research (AJER)
e-ISSN: 2320-0847 p-ISSN : 2320-0936
Volume-6, Issue-6, pp-29-33
www.ajer.org
Research Paper Open Access

An Approach of Improving Performance of the Single Phase AC-DC Sepic Converter

Khadiza Akter[1], Golam Sarowar[2], Dr. Md. Ashraful Hoque[3]
[1](Lecturer, Dept. of EEE, International University of Business Agriculture and Technology, Bangladesh)
[2](Assistant Professor, Dept. of EEE, Islamic University of Technology, Bangladesh) [3](Professor, Dept. of EEE, Islamic University of Technology, Bangladesh)

Abstract: *In this paper new bridgeless Single phase AC-DC sepicconverter with higher efficiency, power factor than conventional sepicconverter is proposed. Conventional AC-DC sepicconverter suffers from demerits like usage of Rectifier Bridge, high diode loss in bridge, low efficiency, low power factor, high THD in input current. Proposed sepicconverter reduces harmonic contamination in power lines; improve transmission efficiency along with power factor correction.*
Keywords: *Bridgeless Rectifier, sepictopology, Power factor Correction (PFC), Total Harmonic Distortion (THD)*

I. INTRODUCTION

Single-phase full wave rectifiers in bridge configuration suffer from problems of non-sinusoidal input current and low input power factor. Various methods have been proposed to solve these problems. One method is to use input filter. Filter inductor and capacitor required in such solution are large. It improves THD but power factor remains low. Significant efforts have been made on the developments of the PFC converters [1]–[4]. As a matter of fact, the PFC circuits are becoming mandatory on single-phase power supplies as more stringent power quality regulations and strict limits on the total Harmonic distortion (THD) of input current are imposed [5].The preferable type of PFC is active PFC since it makes the load behave like a pure resistor, leading to near-unity load power factor and generating negligible harmonics in the input line current [7].Most of the presented bridgeless topologies so far implement a boost-type circuit configuration (also referred to as dual boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. These features have led power supply companies to start looking for bridgeless PFC circuit topologies. In [9], a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. On the other hand, the bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter.

Most active PFC circuits as well as switched-mode power supplies in the market today comprise a front-end bridge rectifier, followed by a high-frequency dc–dc converter such as a boost, a buck–boost, a Cuk, a single-ended primary inductance converter (SEPIC), and a flyback converter. This approach is suitable for a low-to-medium power range. As the power level increases, the high conduction loss caused by the high forward voltage drop of the diode bridge begins to degrade the overall system efficiency, and the heat generated within the bridge rectifier may destroy the individual diodes. Hence, it becomes necessaryto utilize a bridge rectifier with higher current-handling capability or heat-dissipating characteristics. In an effort to improve the power supply efficiency, a number of bridgeless High performance PFC circuit topologies have been proposed [1].Sepic AC-DC converter is a SMPS converter which converts an AC signal to a high level DC signal. Conventional AC-DC Sepicconverter suffers from demerits like usage of Rectifier Bridge, high diode loss in bridge, low efficiency, low power factor, high THD in input current. To reduce harmonic contamination in power lines and to improve transmission efficiency, active power factor correction Many Configurations have been proposed in recent past for improvement of these drawbacks. All these configurations differ in their topology, but all are aiming to more & more possible improvement.

II. PROPOSED CONVERTER

Basic Sepictopology based single phase AC-DC converter that can rectify both positive and negative half cycle of the input individually is shown in Fig. 1. In the positive cycle of the input signal AC-DC conversion is performed through diodes D1, D3and switch S, inductors L1 and L3, capacitors C1 and load RL while during the negative cycle of the input signal diodes D2, D4 switch S, inductors L2 and L4, C2 and load RL are used for the operation of the circuit in Fig. 1 can be explained by splitting it into two different circuits for each positive and negative half cycle.

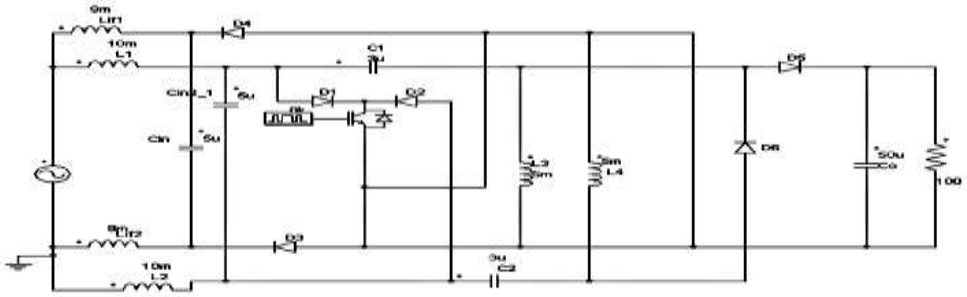

Figure 1: Proposed Sepic Converter

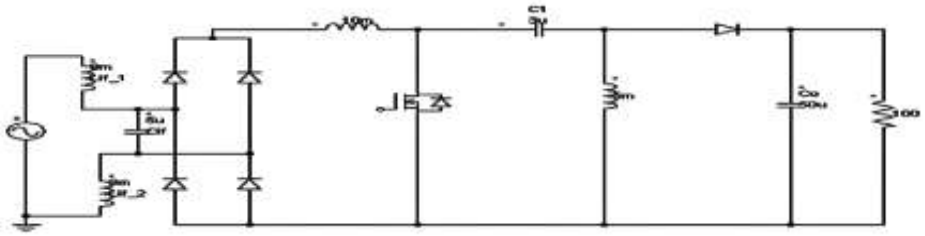

Figure-2: Conventional Sepic Converter

III. PRINCIPLE OF OPERATION

The operations of the proposed circuit in Fig. 3,4,5,6 are explained by four State of conduction along with the direction of current flow. With the switch is at 'ON' and 'OFF' position, the circuit performs AC-DC conversion during positive half cycle of the supply by state 1 and state 2 respectively, while it performs conversion during negative half cycle of the supply by state 3 and state 4 respectively. The principle of operation of the proposed circuit is described below.

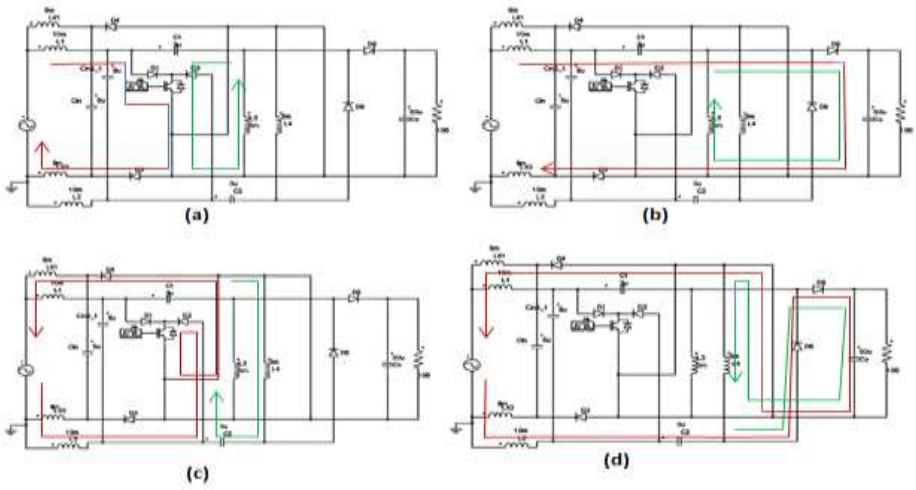

Figure-3: Four modes of operation of proposed Sepic converter. (a) Mode-1: Positive half cycle when switch is ON (b) Mode-2: Positive half cycle when switch is OFF (c) Mode-3: Negative half cycle when switch is ON (d) Mode-4: Negative half cycle when switch is OFF.

State-1: During the positive cycle of the input signal when the switch S is turned on, Current flows in two paths, as shown in Fig. 3. The first is from the input, Inductor L1, through the switch, finally returning back to the input. The second path is from the input, capacitor discharging through the switch, the inductor (L3), and back

to the input.

State-2: In the positive cycle of the input signal when the switch S is non-conducting, the diode D5 is ON. The input capacitors are disconnected, but current continues to flow through the inductors in two paths, as shown in Fig. 3(b). The first is from the output inductor (L3), through the load, and back to the output inductor through the diode D5. The second path is from the inductor (L1), through the energy-transfer capacitor, the diode 5, and back to the inductor (Lif_1).

State-3: Similar to State 1 operation, during the negative cycle of the input signal when the switch S is turned on, the diode D6 is off. Current flows in two paths, as shown in Fig. 3(c)

State-4: In the negative cycle of the input signal when the switch S is turned off and the diode D6 is turned on, current continues to flow through the inductors in two paths, as shown in Fig. 6 like State 2 operation in the positive cycle.

During both positive and negative cycle of the supply, the energy transferred to the load is unidirectional, thus AC-DC conversion is achieved.

IV. SIMULATION

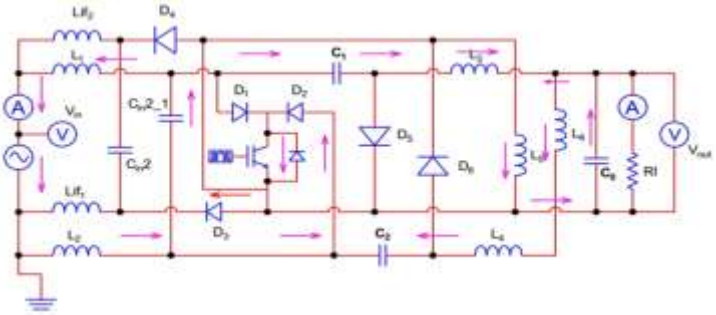

Fig. 4 shows typical waveforms of the input and output voltage for the proposed single phase AC-DC sepicconverter It is evident from the wave shapes that the proposed circuit can effectively improve the performance of the converter.

Table-1: Parameter Table

Parameters	Value
Input voltage (V_i)	220V
Switching Frequency (F_s)	8kHz
Inductor (L_1)	10mH
Inductor ($L_{2,lif1}$)	9mH
Inductor (L_{if2})	9mH
Capacitor (C_1)	3µF
Capacitor (C_2)	3uF
Capacitor (C_{in1})	5 µF
Capacitor (C_{in2})	5 µF
Load across C_0	50uF
Load Resistor	100Ω

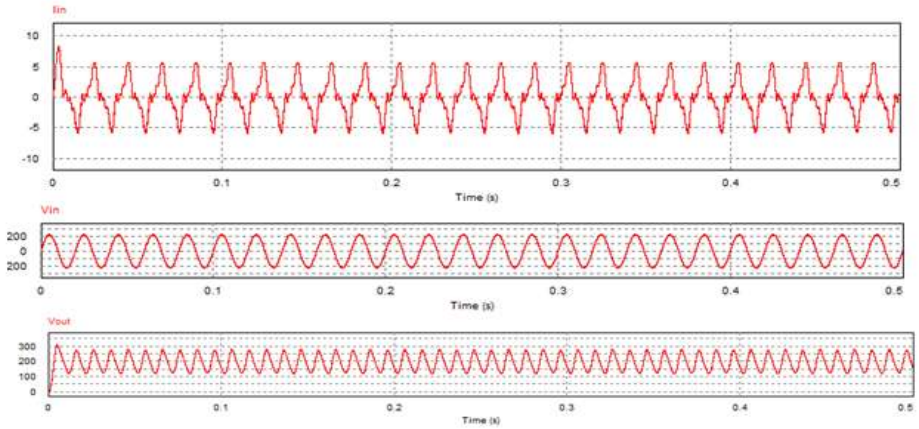

Fig.4: Wave shapes of Input Current, Input Voltage and Output Voltage

V. PERFORMANCE UNDER DUTY CYCLE VARIATION:

Both conventional and proposed single phase AC-DC sepicconverter circuits are subjected to duty cycle variations at a fixed load of 100Ω and constant switching frequency of 8KHz and the performance is monitored in terms of efficiency (%), input power factor, Total Harmonic Distortion (THD) of input current, and voltage gain. The results of these comparisons are presented in Table 2 and in Fig. 5

Table-2: Performance Comparison Table under duty cycle variation

Duty Cycle	Proposed Circuit				Conventional circuit			
	Efficiency (%)	THD (%)	Power Factor	Vgain	Efficiency (%) (%)	THD (%) (%)	Power Factor	Vgain
0.1	87%	76%	0.3	0.25	78%	11%	.63	.16
0.2	96%	56%	0.6	0.39	94%	77%	.77	.34
0.3	97%	39%	0.8	0.59	97%	59%	.84	.58
0.4	98%	41%	0.88	0.9	98%	60%	.85	.89
0.5	99%	42%	0.9	1.3	98%	59%	.858	1.32
0.6	99%	35%	0.9	1.81	97%	50%	.8	1.8
0.7	98%	25%	0.8	2.37	97%	37%	.8	2.5
0.8	98%	11%	0.6	2.78	96%	47%	.8	3.5
0.9	97%	85%	0.35	2.9	96%	48%	.8	7.3

The performance of the circuits in terms of efficiency (%) is presented by the bar diagram as illustrated in Fig. 5(a). The proposed circuit shows good performance offering more than 92% efficiency throughout the range of duty cycle. From the line chart in Fig. 5(d) showing percent Total harmonic distortion (THD) of input current demonstrates better performance of the proposed scheme over the conventional one. All through the operation of the proposed circuit the

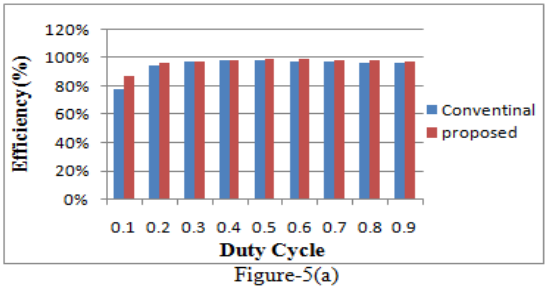

Figure-5(a)

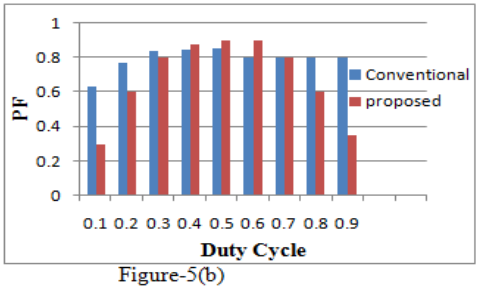

Figure-5(b)

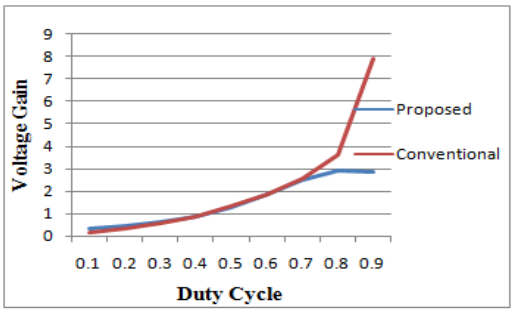

Figure-5(c)

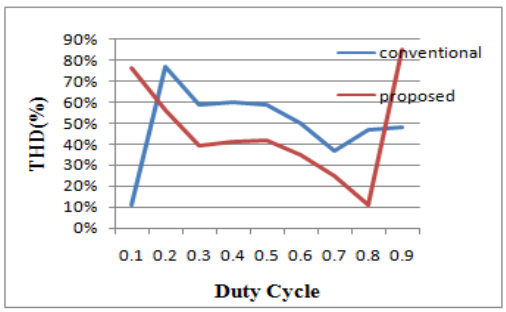

Figure-5(d)

THD (%) was found better. The proposed converter presents higher voltage gain than the conventional circuit all over the duty cycle as illustrated in the line chart presented in Fig. 5(c). Input power factor comparison as shown in the overlaying bar diagram in Fig. 5(b) indicates that the proposed scheme is competitive providing near unity power factor during duty cycle variations except at D = 0.9 where performance of both schemes is not good.

Table-3: Performance Comparison Table under load variation

		Proposed Circuit			Conventional Circuit	
Load	Efficiency (%)	THD (%)	Power Factor	Efficiency (%)	THD (%)	Power Factor
10	85%	2%	0.9	98%	12%	.2
20	99%	12%	0.9	99%	8%	.9
30	99%	24%	0.9	99%	21%	.9
40	99%	33%	.9	99%	28%	.9
50	99%	40%	0.9	99%	34%	.9
60	99%	43%	0.8	99%	39%	.9
70	99%	42%	0.8	99%	39%	.9
80	99%	45%	0.8	98%	43%	.9
90	99%	44%	0.8	98%	45%	.9
100	99%	43%	0.8	98%	46%	.9

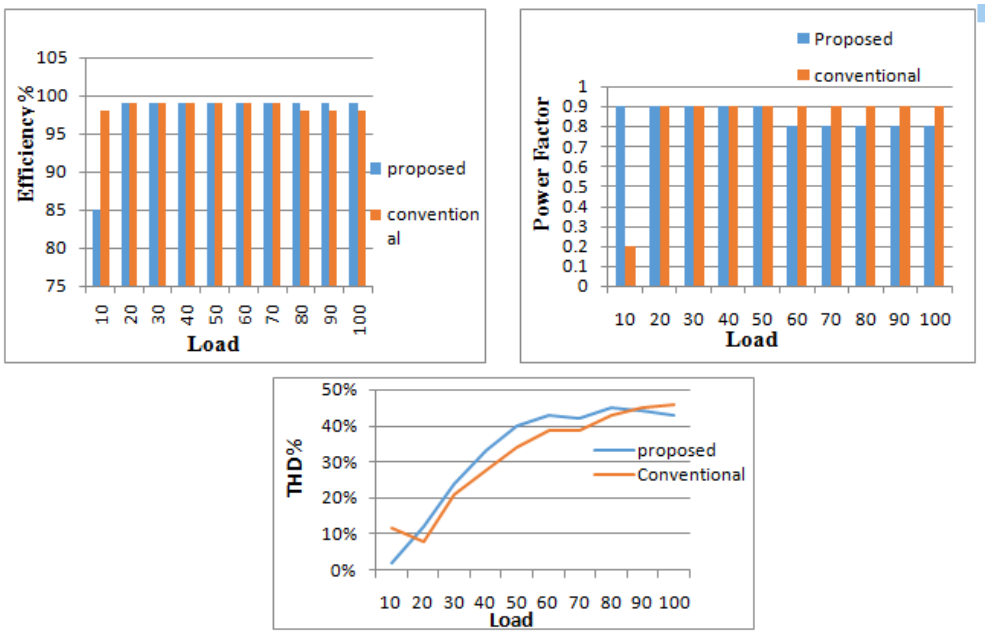

Figure-6: Efficiency, Input current THD and power factor comparison for proposed AC-DC Sepic with Conventional Sepic converter under load variation

VI. CONCLUSION

In this paper, a simple single-phase bridgeless sepicrectifier with low input current distortion and high efficiency has been proposed and verified. The proposed bridgeless topology is derived from the conventional Sepic and Cuk converters. Comparing with conventional Sepic and Cuk PFC circuit the circuit chops the input current at the AC side in contrast to the conventional design which chops the rectified output. Comparisons are made between the proposed topology and the conventional Cuk. The proposed scheme demonstrates better performance having low input current THD, high power factor and high efficiency. Moreover, it does not require any additional control schemes in order to reduce the harmonics. Based on the results obtained from simulation, the proposed scheme can be considered for AC-DC conversions with low distortion and high input power factor and efficiency.

REFERENCES

[1]. M.R.T. Hossain, M. H. Rahaman, M. S.Arifin, M. A Choudhury. A.H.Abedin,M.N.Uddin,"Input Switched Single Phase High Performance Bridgeless AC-DC Zeta Converter", IEEE International Conference on Power Electronics, Drives and Energy Systems, December16-19, 2012,

[2]. O. Gracia, J. A. Cobos, R. Prieto, and J. Uceda, "Single phase power factor correction: A survey," IEEE Trans. Power Electron., vol. 18, no. 3,749–755, May 2003

[3]. B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters", IEEE Transactions on Industrial Electronics, Vol. 50, No. 5, Oct. 2003, pp 962 – 981.

[4]. R. Martinez and P. N. Enjeti, "A high performance single phase rectifier with input power factor correction," *IEEE Trans. PowerElectron.*, vol. 11, pp. 746-752, pp. 311-317, Mar. 1996

[5]. M. Brkovic and S. Cuk, "Input current shaper using Cuk converter," in *Proc. Int. Telecommun. Energy Conf.*, 1992, pp. 532–53

[6]. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses", IEEE Transactions on Industry Applications, Vol. 47, No. 2, March/April 2011, pp. 873-881.

[7]. H. Ismail, "Bridgeless SEPIC Rectifier with Unity Power Factor and Reduced Conduction Losses", IEEE Transactions on Industrial Electronics, Vol. 56, No. 4, April 2009, pp. 1147-1157.

[8]. Abbas A. Fardoun, Esam H. Ismail, Ahmad J. Sabzali and Mustafa A. Al-Saffar, "New Efficient Bridgeless Cuk Rectifiers for PFC Applications," IEEE transactions on power electronics, vol. 27, no. 7, July 2012

[9]. L. Huber, Y. Jang, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Trans. Power Electron.*, vol. 23, pp. 1381-1390, May 2008.