American Journal of Engineering Research (AJER) 2016
American Journal of Engineering Research (AJER)
e-ISSN: 2320-0847 p-ISSN : 2320-0936
Volume-5, Issue-11, pp-297-305
www.ajer.org
Research Paper Open Access

An Improved Active Filter Technique for Power Quality Control under Unbalanced Dynamic Load Condition

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ABSTRACT: *This paper presented an improved approach for active filtering topology using simplified multi-level inverter. The modified phase opposition disposition (MPOD) scheme is presented on simplified multilevel inverter. The multilevel inverter obtained 9 level injecting power using 12 active power switches. The Modified POD scheme has a single carrier and multi-reference signal for PWM implementation for presented active filter topology. The enhanced reference frame method is used in PWM generation so that it is not required auxiliary elements for improving power quality and eliminating the higher order harmonics. The enhancement of this scheme is obviously verified under unbalancing load and dynamic load conditions. The comparison with five level injected schemes, the present scheme has better result in the form of harmonics elimination, power factor improvement and reactive power compensation.*

Keywords: *Mat lab, MRFC, PFC, PWM, THD*

I. INTRODUCTION

The study and focusing of power quality is an important ingredient in electrical field to maintaining and improving the power quality. The power converter has provides a crucial role for focusing in power quality. The power converter is basically has a non-linear property and it's drawn a saturated power in input supply and load [1]. Power converter injects line across the point of common coupling (PCC) in between supply to load. The classical approach for power quality improvement or power quality standard are the passive elements such as capacitor, inductor. Classical scheme has bad mark on bulky in size, fixed solution for compensation, resonance problem and electromagnetic intrusion [2].

The active power filter is an advanced technique for improving power quality or maintaining the power quality as per the standard limits [3]. The multilevel inverter is recently developed for medium to high power application under power quality standard. Multilevel inverter topology Applied in electrical drives control and reactive power elimination. The multilevel inverter stands for low power rating of power switches and passive elements, suppressing Total Harmonics Distortion (THD) across the load. The Pulse Width Modulation (PWM) generation and implementation is for multilevel inverter. This PWM implementation is because of resolving semiconductor or power switch limitation [4],[5].

The enhancement of multilevel inverter has reaches the necessities such as generate a pure angle of sinusoidal injected voltage and low Total Harmonics Distortion (THD) of load current by present inverter. The classical approach of three-level and five-level inverter cascaded and flying capacitor type and it has required excessive filters and excessive ranges for meet out necessities. So lower frequency and lower rating of power switches used in enhancement of present simplified multilevel inverter based active filter topology shown in Fig.1. The present scheme has low power losses, capable of reactive power elimination, power factor correction by simplified structure and modified phase opposition and disposition scheme. The present scheme is applied under non-linear load, dynamic load and unbalancing load conditions and verified by using simulation results.

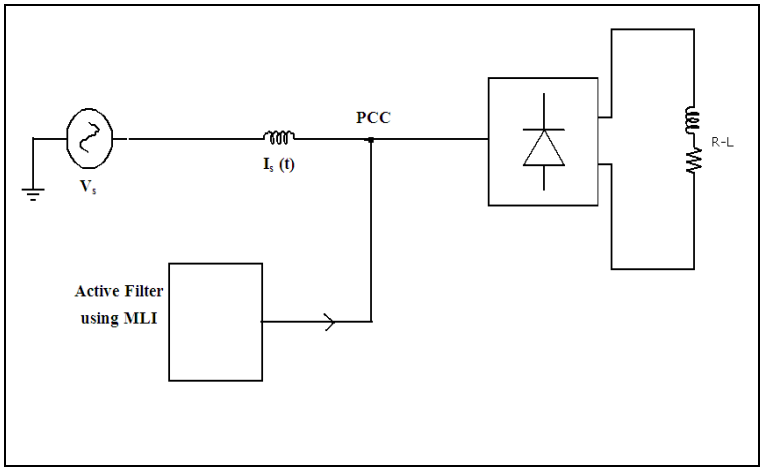


Fig. 1. The basic configuration of Active filter topology

II. THEBASIC CONFIGURATION OF ACTIVE FILTER

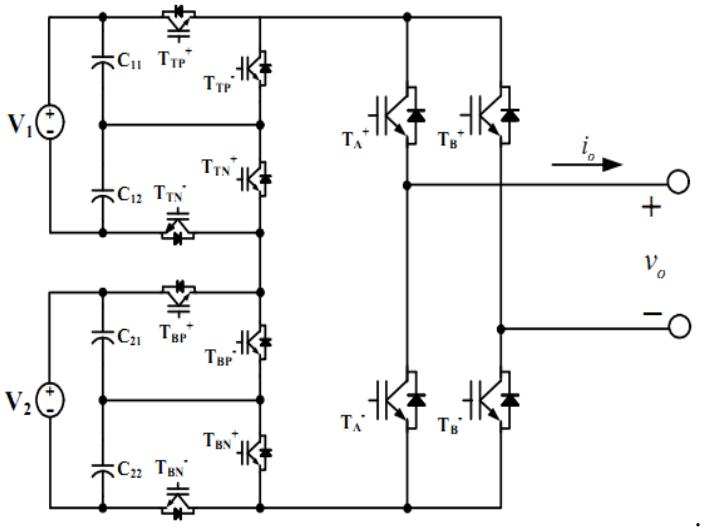
The active filter is injecting current in quadrature form and opposite to harmonics across the point of common coupling. The injected current from active filter called compensation current. The harmonics generation and reactance is generated by non-linear, unbalancing and dynamic load conditions. So pulse width modulation based power converter is applied as active filter topology which is shown in Fig.1.

The basic nature of multilevel inverter is not requires a coupling transformer and injected excessive passive elements. The modified phase opposition and disposition is used in present active filter topology for controlling current and harmonics suppression shown in Fig. 2.

III. THE ACTIVE POWER FILTER TOPOLOGY USING SIMPLIFIED MULTILEVEL INVERTER

Output voltage(Vo)	Switching condition					
	S_{P1}	S_{P2}	S_{N1}	S_{N2}	S_{A1},S_{B2}	S_{A2},S_{B1}
V_{DC}	ON	OFF	OFF	ON	ON	OFF
$\frac{V_{DC}}{2}$	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
$\frac{-V_{DC}}{2}$	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
$-V_{DC}$	ON	OFF	OFF	ON	OFF	ON

IV. THE ACTIVE POWER FILTER TOPOLOGY USING SIMPLIFIED MULTILEVEL INVERTER



Output voltage(Vo)	Switching condition					
	S_{P1}	S_{P2}	S_{N1}	S_{N2}	S_{A1},S_{B2}	S_{A2},S_{B1}
V_{DC}	ON	OFF	OFF	ON	ON	OFF
$\frac{V_{DC}}{2}$	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
$\frac{-V_{DC}}{2}$	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
$-V_{DC}$	ON	OFF	OFF	ON	OFF	ON

V. MODES OF OPERATION OF ACTIVE POWER CONVERTER

The proposed PWM method has five levels (V_{DC},$V_{DC/2}$, 0,$-V_{DC/2}$,$-V_{DC}$) as per to the switching mode of the inverter. There are four manners of working submit the rapid value of reference and outside value of the carrier signalV_C. Inverter output voltage drawn through operating ranges shown in Table II.

The Novel pulse width modulation approach based on pod (phase opposition and disposition) modulation requires only a single carrier ($V_{carrier}$). It is proposed the detailed PWM strategy is represented in fig. 3

If the reference signal is positive, then the switch pair (S_{A1},S_{B2}) are turn on, and if reference is negative, then the switching pairs (S_{A2},S_{B1}) are turn on.

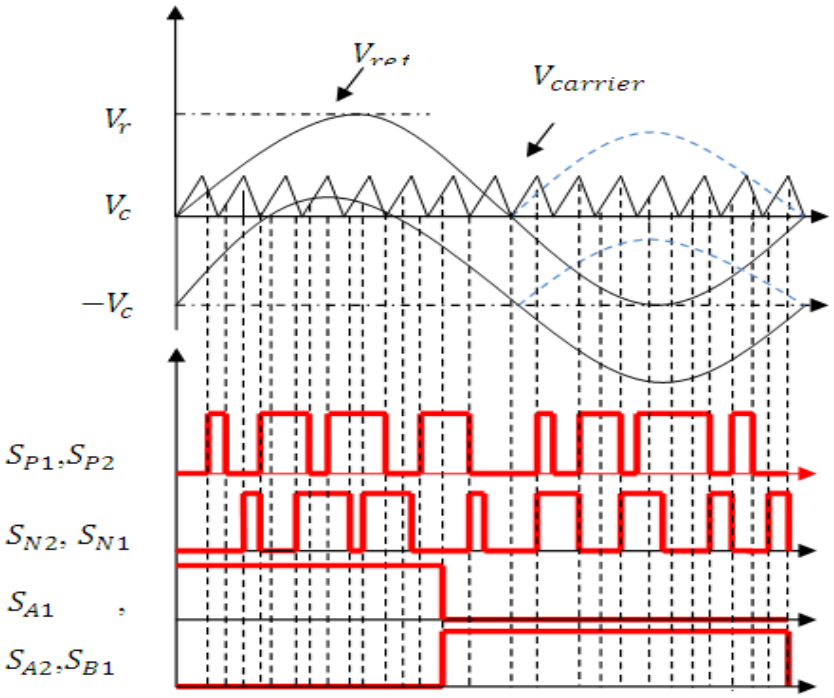


Fig. 3. PWM strategy based on MPOD with single carrier signal

Thus the switches composing the H bridge inverter turned on and turn off once during the period of the reference signal. The voltage across the switch at blocking state is V_{DC} .the switches (S_{P2},S_{N1}) are operated complimentary to the switches (S_{P1},S_{N2}).The PWM signal generates for proposed module can be explained as follows:

Mode 1: A signal withholds from the reference signal by V_c is compared with the carrier signal. If V_{ref} - V_c>$V_{carriers}$ then all switches S_{P1} or S_{N2} are turned on. If V_{ref}-V_c<$V_{carriers}$, then the switch S_{P1} or S_{N2} is turn off alternately and current flow through Diodes (D_{in} ,D_s,D_5D_6)and B_{SW1} are ON .thenD_1,D_2,D_4 are OFF. Charging and discharging of Inductors (L_1,L_2,L_3,L_4,L_5) continuously. Capacitor start to charge (C_1andC_2).

Mode 2: the reference signal is directly compared with a carrier signal. If V_{ref}>$V_{carriers}$ then the switch S_{P1} or S_{N2} is turned on alternately. If V_{ref} < $V_{carriers}$ then all switches S_{P1} and S_{N2} are turned off. ThenD_{in}, D_s,D_3, D_5 and D_6 and B_{SW1} are ON. Then D_1 , D_2 , D_4 are OFF. L_1 , L_3 , L_4 , L_5 is charged by Supply (V_{in}) C_1 and C_2 are continuous to charge.

Mode 3:V_{ref} directly compared with a carrier signal. If V_{ref}>$V_{carriers}$ then the switch S_{P1} or S_{N2} is turned on alternately. If $-V_{ref}$<$V_{carriers}$ then all switches S_{P1} and S_{N2} are turned off. ThenD_{in} D_s,D_3,D_5,D_6 and $B_{SW1}$are ON. ThenD_1,D_2,D_4 are OFF.L_1,L_2, L_3,L_4,L_5 is charged by $C_1$and C_2.

Mode 4: a signal subtracted from $-V_{ref}$ by V_C is compare with carrier signal. If $-V_{ref}$-V_c>$V_{carriers}$ then all switches $S_{P1}$and S_{N2} are turned on. If $-V_{ref}$-V_c<$V_{carriers}$ then the switch S_{P1} or S_{N2} is turned off alternately. $D_{in}$$D_s$,$D_3$,$D_5$,$D_6$ and $B_{SW1}$are ON. ThenD_1,D_2,D_4 are OFF.L_1,L_2, L_3,L_4,L_5 is charged by C_1andC_2.

TABLE II: Operating mode of proposed MLI

Operating mode	Reference voltage range	Output voltage
Mode 1	$V_C \le V_{ref} < 2V_C$	$V_{DC}/2$ or V_{DC}
Mode 2	$0 \le V_{ref} < V_C$	0 or V_{DC}
Mode 3	$-V_C \le V_{ref} < 0$	$-V_{DC}/2$ or 0
Mode 4	$-2V_{DC} \le V_{ref} < -V_C$	$-V_{DC}$ or $-V_{DC}/2$

VI. CONTROL STRATEGY

The main aim of the control strategy is to maintain power quality as in standard limits. The system control is used to maintain desired range of power quality under unbalanced dynamic load condition. The Active Filter is compensating reactance value but voltage ripple and current ripple is need to be reduce then easily power factor correction is reduces. Therefore the APF needs very sensible controller and circuits.

a) Modified Synchronous Reference Frame Control (MRFC)

In traditional topology there are so many active filtering methods such as reactive power control theory (p-q theory), unity power factor control, one cycle control and Fast Fourier Technique etc. the proposed scheme has used to extract the reference current generation using active filtering [6].The presented modified synchronous reference frame (MSRF) explain about harmonics and extract the harmonics component. The source current of and is detected and is transferred in to two-phase stationary frame from stationary reference frame. The detection scheme has been made by the following equation

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

The two phase stationary reference frame of and is transformed into direct and quadrature axis frame by equation (2). The cosine and sine angle are generated using phase lock loop (PLL) reference frame.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (2)$$

The generation of dq-currents obtained by incorporated of AC and DC parts. The fundamental component of fixed DC and AC parts represents the harmonics component. The harmonics or current transient can be easily extracted using low pass filter shown in fig.4

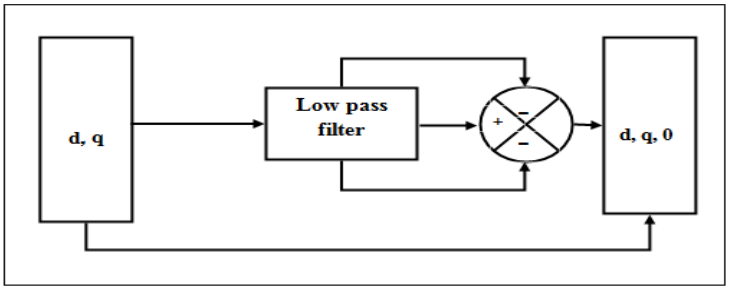


Fig.4 the block diagram for MSRF algorithm

The direct axis current is obtained from combination of active fundamental current and load current harmonics .The fundamental component is represents in synchronous reference frame. The direct axis component of harmonics is obtained by subtracting from it is presented in load. Quadrature axis harmonics current obtained by sum of reactive form of load current and load harmonics.

The and reference frame is generated by following equation

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{dh} \\ i_q \end{bmatrix} \quad (3)$$

The reference current $(i_a{}^*, i_b{}^*, i_c{}^*)$ of are obtained by the following expression

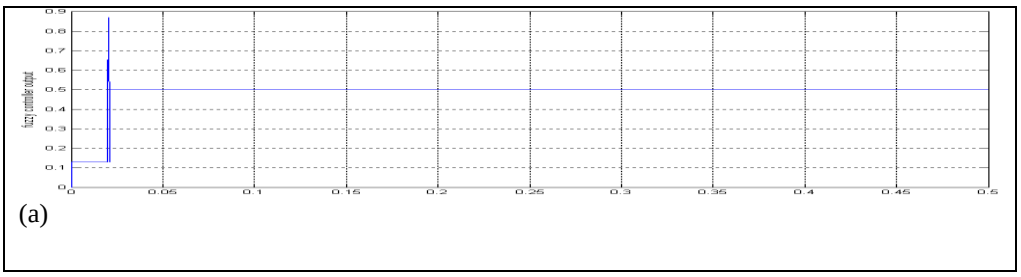
$$\begin{bmatrix} i_{ca}{}^* \\ i_{cb}{}^* \\ i_c{}^* \end{bmatrix} = [T_{abc}] \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad (4)$$

$$[T_{abc}] = \sqrt{2/3} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \quad (5)$$

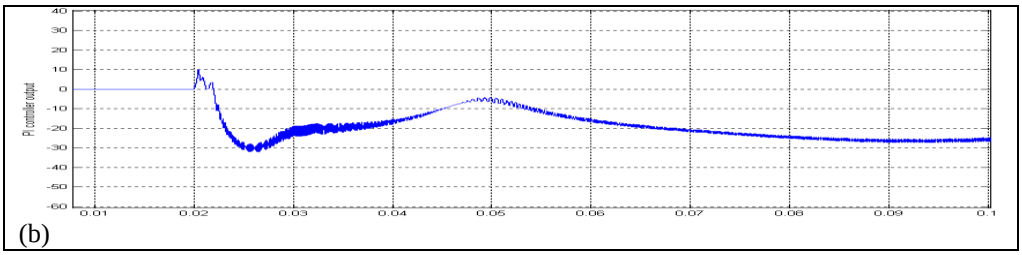
b) Fuzzy logic controller scheme

The effective Active Filter is adapted with simplified 9- level Inverter system. The basic nature of dynamic voltage restorer injects the reactance to suppress the reactive power which is generated in load [7] and also observed harmonics and current transient problem. The main demerit of PI controller is its incompetence in precipitate conditions of error signals, ε , because it can consider the value of signal alone except the change of rising and falling time, i.e derivative error signal, $\Delta\varepsilon$. To solve power quality problem, a smooth waveform is achieved using proposed fuzzy logic scheme. The presented fuzzy logic scheme is based on Mamdani's system and it is used to improve the fast transient performance in phase lock loop control circuit. The fast transient performance of fuzzy logic controller over PI controller is shown in Fig.5.

The fuzzy control system as shown in Fig. 6 consists of fuzzification, defuzzification and decision making stage [8]. The proposed fuzzy logic controller applied in phase lock loop reference schemes for improving the angle control [9] and supplying to effective alpha, beta and d-q reference current generation. The fuzzy based PLL provides fast transient performance over the PI based PLL controller. The proposal of fuzzy logic scheme has the capability to extract the harmonics current from actual current signal and it is provided the suitable reference signal generation for pulse generation of active dynamic voltage restorer. The modified reference frame controller has provided satisfactory reference signal by crucial appearance of fuzzy logic PLL scheme and fuzzy rules is shown in Fig. 6.



(a)



(b)

Fig. 5 controller comparison performance: (a) fuzzy controller on APF. (b) PI controller on APF

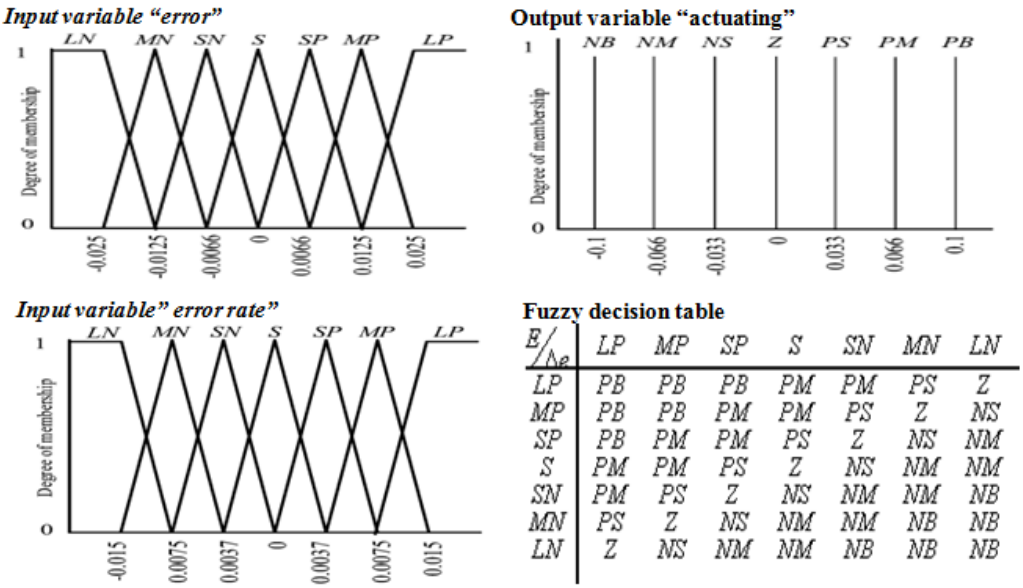


Fig. 6 Membership functions of I/O fuzzy sets and control rules assignment.

VII. SIMULATION RESULTS AND DISCUSSION

The enhancement of proposed scheme has ability to control power quality in the form of reactive power compensation across load, improving the real power, Total Harmonics Distortion (THD) elimination and power factor correction. The present improved multilevel inverter topology based Active filter is provided a maximum level of harmonics elimination over 5-level approach is shown in Figure.7. The present system is analysis under Non-linear and Dynamic load condition. The ripple power is identified and controlled by active modified reference frame controller.

The controller is proved as a better and also prominent solution for controlling ripple content present which Non-Linear and Dynamic load. The simulation implementation and it is verified by MATLAB/Simulink software. The enhancement of modified phase opposition and disposition controller is implemented using improved form of reference frame controller. Reference frame controller is played an important role in harmonics reduction. MSRF via extracting ripple current and can

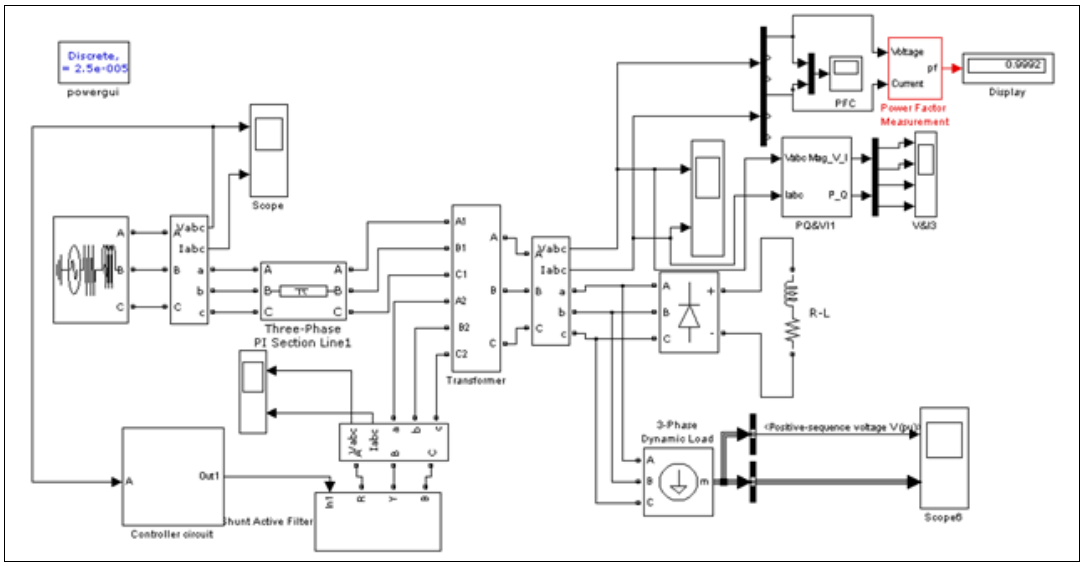


Fig.7 simulation circuit implementation of proposed scheme

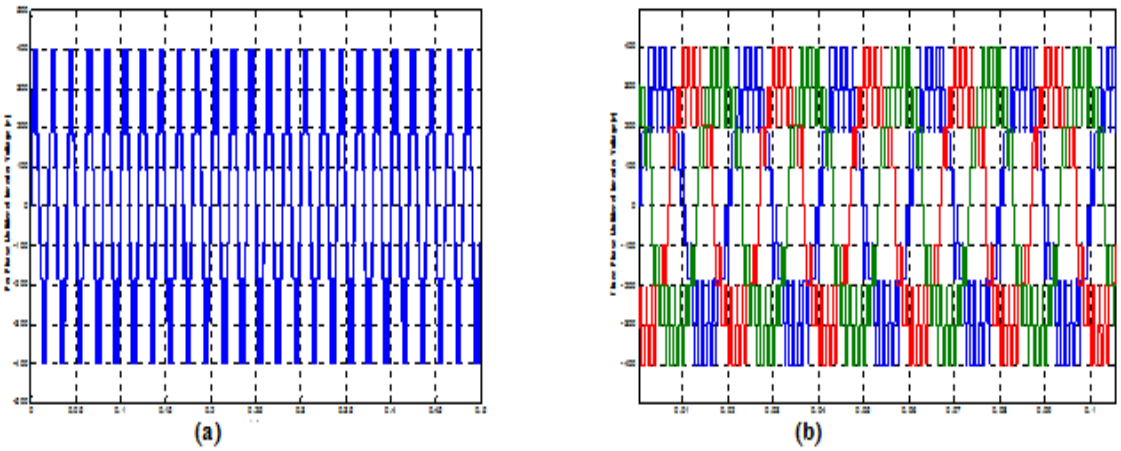


Fig.8 Simplified Multilevel Inverter Performance: (a) Per-Phase Inverter Voltage. (b) Three- Phase Multilevel Inverter voltage.

The present multilevel inverter is obtained Nine-Level voltage to reduce and improving the active filter performance. The performance of per-phase voltage and Three-phase voltage is shown in Figure.8. Testing of this system is required low ranges of passive elements and by the passive elements R-C circuits used to draw the injected voltage which is shown in Figure. 9(a). The power quality improved performances are shown in Figure from 9(b) to 9(d). The total harmonics distortion is obtained and this is proved as a better scheme over existing Five-level approach is shown in Figure.10 and desired standard limits [10]. By the way power factor correction is reached 0.9

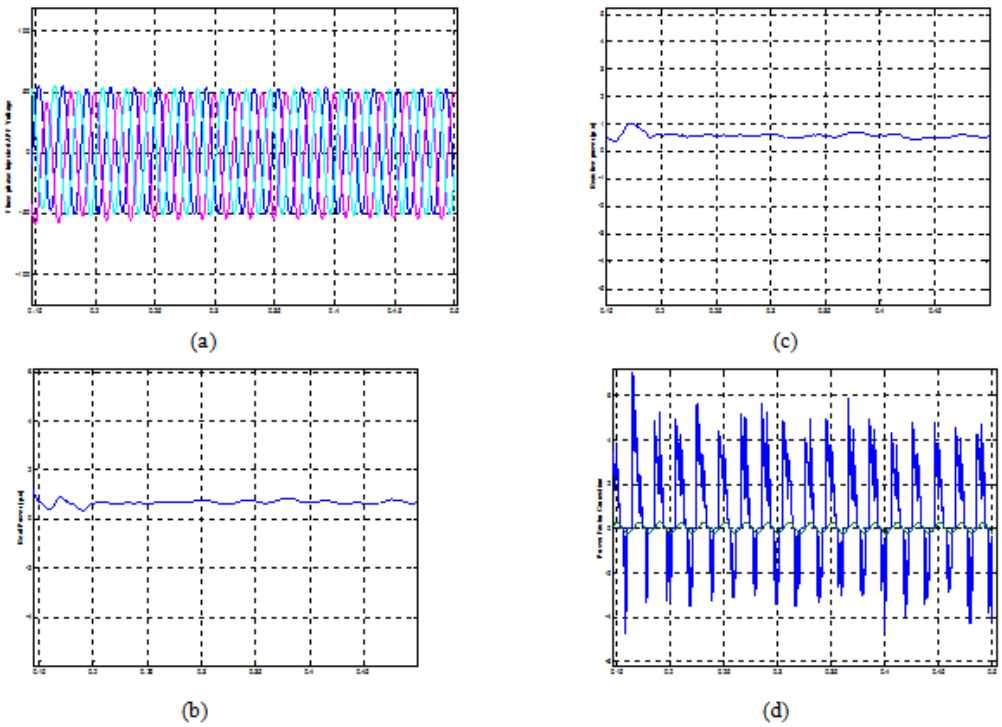


Fig.9 Power quality performance of proposed system: (a) Injected Voltage. (b) Real Power (P). (c) Reactive Power (Q). (d) Power Factor Correction

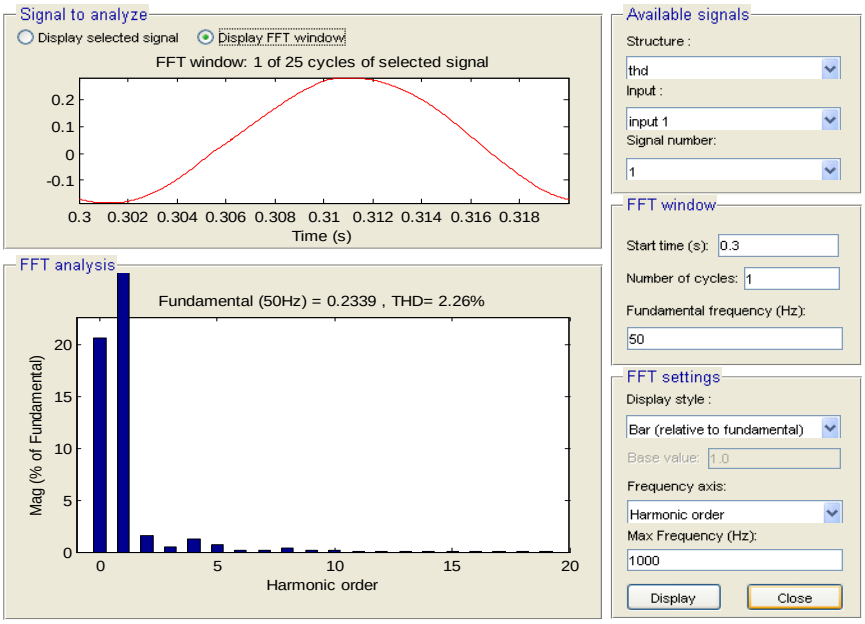


fig.10. TotalHarmonics Harmonic Distortion (THD) using FFT met

REFERENCES

[1] Rani, K. Sebasthi, and K. Porkumaran. "Multilevel shunt active filter based on sinusoidal subtraction methods under different load conditions." Computational Technologies in Electrical and Electronics Engineering (SIBIRCON), 2010 IEEE Region 8 International Conference on. IEEE, 2010.

[2] B. Singh. K. Al-Haddad and A. Chandra, "A review of active filters for power quality improvement," IEEE Transactions on Industrial Electronics. Vol. 46. No. 5, pp. 960-971, October 1999.

[3] Zellouma, L., and S. Saad. "Three-Level Shunt Active Filter Compensating Harmonics and Reactive Power."2006.

[4] B.-R. Lin, T.-Y. Yang, "Three-level voltage-source inverter for shunt active filter", IEE, Electric Power Applications, pp.744–751, Nov.2004.

[5] B.-R. Lin, H. K. Chiang, C.-H. Huang, "Three-phase three-level active power filter with a clamped capacitor topology", IEE, Electric Power Applications, pp.513 – 522, July 2006.

[6] E. J. Acordi, A. Goedtel. and L. C. B. Nascimento, "A Study of Shunt Active Power Filters Applied to Three-Phase Four-Wire Systems", ICREPQ'12 - Spain, 28 - 30 March, 2012.

[7] Yu Jiang , Heping Liu, QunyingZheng , LianqingZheng" A Novel Apparatus for Adjusting the Insertion Voltage of Transmission Line Based on Variable Inductors"IEEE trans., on power delivery, Vol.27 , Issue. 1, Jan. 2012.

[8] AhmetTeke, LütfüSaribulut, and Mehmet Tümay" A Novel Reference Signal Generation Method for Power-Quality Improvement of Unified Power-Quality Conditioner" IEEE Transactions on Power Delivery, Vol. 26, No. 4, Oct.2011

[9] Ahmad Osman Ibrahim, ThanhHai Nguyen, Dong-Choon Lee and Su-Chang Kim "A Fault Ride-Through Technique of DFIG Wind Turbine Systems Using Dynamic Voltage Restorers" IEEE Trans., On Energy Conversion, Vol. 26, No. 3, Sept.2011

[10] Duffey, Christopher K., and Ray P. Stratford. "Update of harmonic standard IEEE-519: IEEE recommended practices and requirements for harmonic control in electric power systems." Industry Applications, IEEE Transactions on 25.6 (1989): 1025-1034.