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Design of a PWM for UPS with Pulse Dead Time

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ABSTRACT : *This paper presents a new design of a power width modulator PWM with and without dead time for each PWM pulses based on specific criteria given. In order to study and design a new model of PMW Inverter and to show the effects of dead time on the PWM which was designed and achieved. In this paper, comparison between PWM with &without dead time. The design methodology comprises of the calculations and results analysis. P-Spice simulator was used as a tool to verify the results. The effectiveness of the proposed technique was confirmed. All the waveforms voltage, current, and power achieved and discussed.*
Keywords – *PWM, Modeling, power electronics design, Harmonics elimination, and inverters.*

I. INTRODUCTION

One of the main problems encountered in open-loop pulse width modulation inverter (PWM) drives is the nonlinear voltage gain caused by the non ideal characteristics of the power inverter. The most important nonlinearity is introduced by the necessary blanking time to avoid the so-called shoot through of the dc link. To guarantee that both switches in an inverter leg never conduct simultaneously a small time delay is added to the gate signal of the turning-on device.

This delay, added to the device's finite turn-on and turn-off times, introduces a load dependent magnitude and phase error in the output voltage. Since the delay occurs in every PWM carrier cycle the magnitude of the error grows in inverse proportion to the output fundamental frequency, introducing a serious waveform distortion and fundamental voltage drop The voltage distortion increases with switching frequency introducing harmonic components that, if not compensated, may cause instabilities as well as additional losses in the machine being driven[1].

The output voltage distortion is the finite voltage drop across the switches during the on state the dead time necessary to prevent the short circuit of the power supply in pulse width modulated (PWM) voltage inverters results in output voltage deviations. Although individually small, when accumulated over an operating cycle, the voltage deviations are sufficient to distort the applied PWM signal [2].

The top and bottom switch has to be "complementary", i.e. if the top switch is closed (on), the bottom must be off, and vice-versa. In practical, a dead time as showed below is required to avoid "shoot-through" faults as showed in Fig.(1)[3].

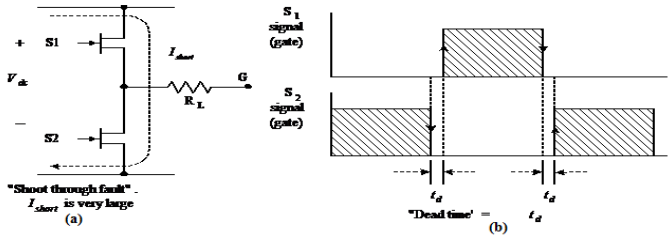

Fig.1 a) Shoot through fault, b) Dead time waveform

Based on various circuit topologies and modulation strategies have been reported for better utilization of multilevel voltage source inverters. Multilevel topologies are classified in to three categories: diode clamped inverters, flying capacitor inverters and cascaded inverters. The topologies have an equal number of main switches[4].

The diode clamped inverter uses a single dc bus that is subdivided in to number of voltage levels by a series string of capacitors. A matrix of semiconductor switches and diodes allows each phase leg output to be switched to any of these voltage levels. The main drawback of diode clamped inverter is the unbalanced dc link capacitor. It restricts the application of diode clamped inverter to five or less number of levels. Flying capacitor inverter requires the most number of capacitors [5-6].

Finally, in this paper design of a power width modulator PWM with dead time for each PWM pulses based on specific criteria given. In order to analyse the effects of dead time insertion to PWM inverter, and To know how to design rectifiers for electronic devices (UPS). All techniques for the analysis and design of rectifiers through simulation were achieved[7].

II. PULSE WIDTH MODULATION

Fig.(2) shows the PWM is the most popular method for producing a controlled output for inverters. They are quite popular in industrial applications[8-9].

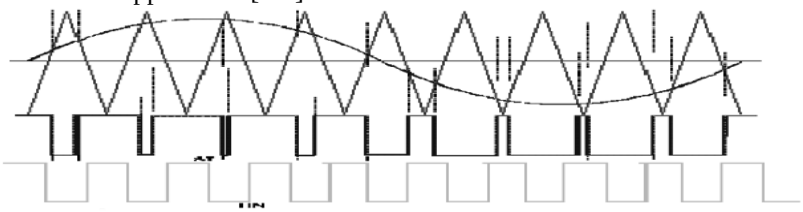

Fig.2 (sine modulated, unmodulated signal)

III. METHODOLOGY

The Methodology of this paper consist of five main stages. As following :
Stage1: design of inverter concept based on theories study.
Stage 2: simulation of the inverter circuit by PSPICE simulator.
Stage3: design & development of the switching pulse based on simulation and calculation.
Stage4: development of single phase inverter, fine, tuning, and testing.
Stage 5: Input data get results monitoring and conclusion.

IV. DESIGN and CONSIDERATIONS

Two designs was considered in this paper the power width modulator PWM with and without dead time with specific criteria as shown:
1) Input voltage: 24V Battery bank
2) Output voltage: 240Vrms + 5%
3) Output power: 500 W
4) Voltage THD < 5%

The amplitude of the PWM of the fundamental frequency output is controlled by ma . This is significant for an unregulated DC voltage because the value of ma can be adjusted to compensate the variations in the DC voltage, thus producing a constant amplitude output. When ma is greater than 1 or over modulation, the amplitude of the output increases with ma , but not linear.

$Mf = f_{carrier} / f_{ref}$. (1)

Where;
fcarrier = ftri =Triangular carrier waveform frequency.
freference = fsin = Fundamental waveform frequency.

$Ma = V_{m,ref} / V_{m,carrier}$ (2)

Where;
Vm,reference = Vm,sin = Peak amplitude of reference waveform.
Vm,carrier = Peak amplitude of triangular carrier waveform.

V. SIMULATION RESULTS

A. PWM inverter without dead time

Figure(3) shows the Circuit diagram of PWM inverter with dead time. Consist of four switches and two comparators with R load.

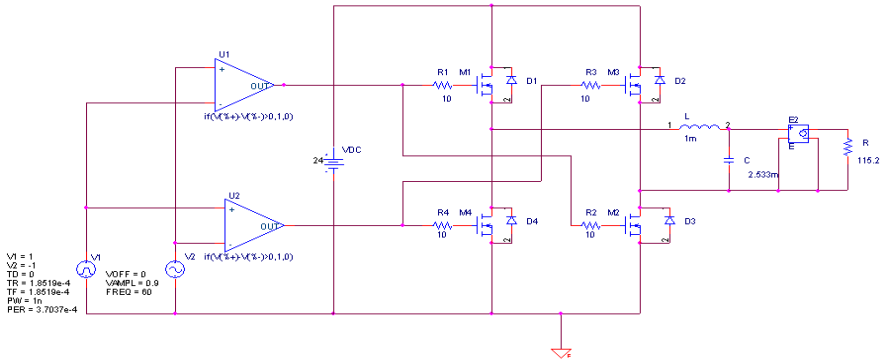

Fig.3 Circuit diagram of PWM inverter without dead time.

Fig. (4) shows the voltage output waveform. From the reading shown that the voltage output is 341.698V. The result shown meet the requirement for the design specification where the design need 240V_{rms} voltage output.

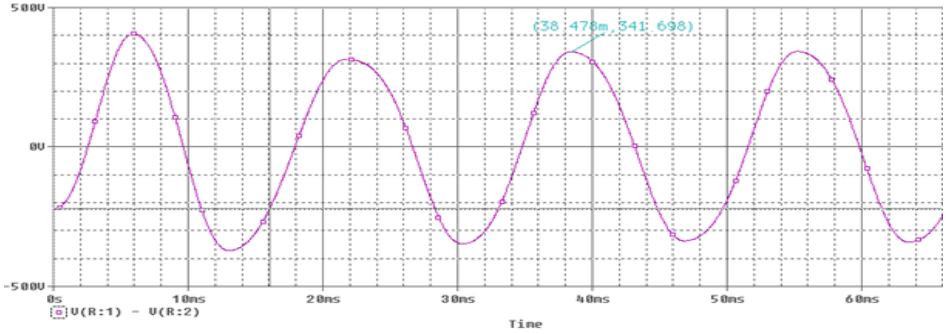

Fig.4 Inverter output voltage.

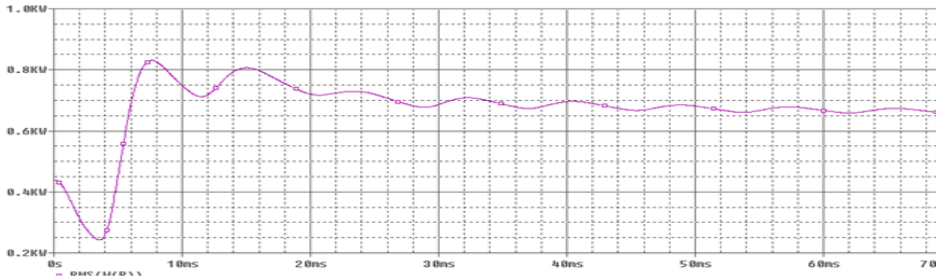

Fig. 5 Power output.

The power is going to stabilize around 650W. The time for the graph cannot be increased anymore because convergence will occurred. After checking with the voltage output, the V_{rms} value is 251. 458 as shown in Fig.(5). By using the formula for the power,

$P=V_{rms}^2/R$ (3)

The calculated power is 550W and this met the requirement for the power output. Fig.(5) shows the waveform for the PWM output. Waveform for the output V_{rms} value as shown in the Fig.(6)

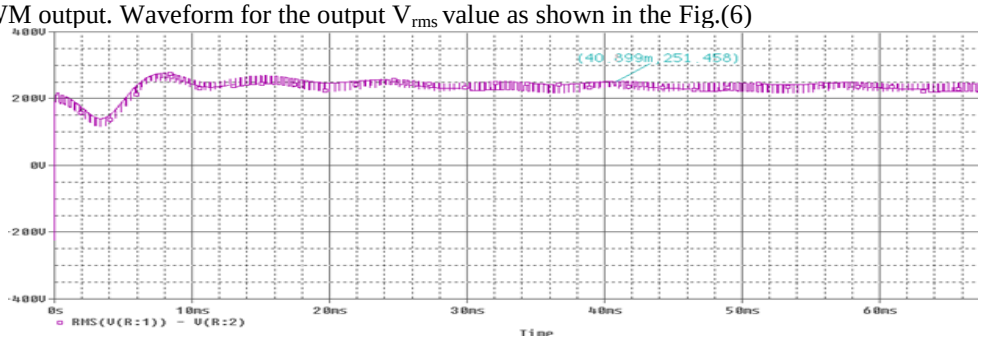

Fig.6 Waveform for the output V_{rms} value.

Fig. (7&8) shows the switches pulses. Two switches work at time.

Fig. 7 S1&S3 pluses

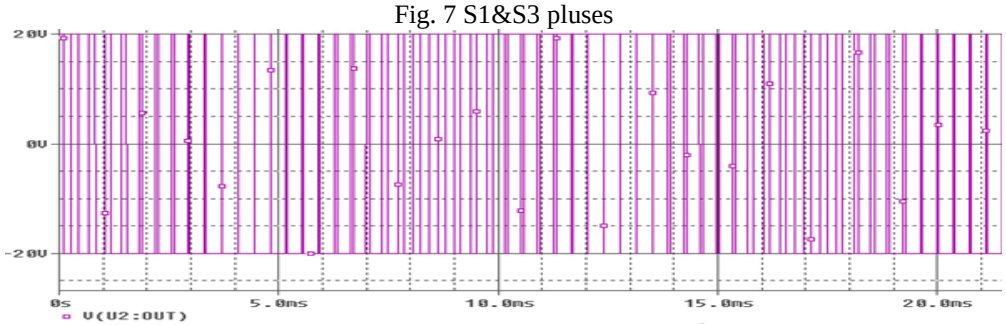

Fig.8 S2&S4 pluses

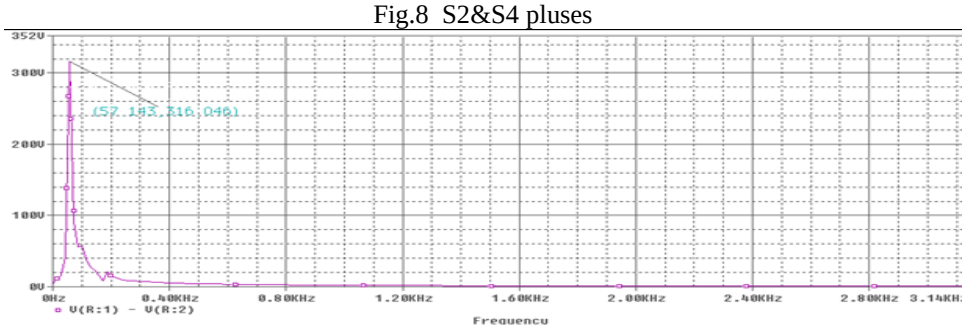

Fig.9 Harmonic frequency.

In Fig.(9) , the Fourier series for the voltage output is shown. To find the first harmonic frequency, the formula used is

$f=kM_Rf_m$ (4)

Where

k is the number of the harmonic will occur, M_R is the modulation ratio and f_m is the modulating frequency. The first harmonics will occur at frequency, 2.7kHz and from the waveform there are no harmonics at that frequency. So we can conclude that the total harmonic for this circuit is below than 5 percent.

B. PWM inverter with dead time

Figure(10) Circuit diagram of PWM inverter with dead time. This design analyzes the effects of dead time insertion to PWM inverter. The dead time between switching pulse for both set of MOSFET (M1, M2 and M3, M4) is 1µs. dead times must be inserted before turning on the switch to avoid simultaneous conduction and shoot-through problems.

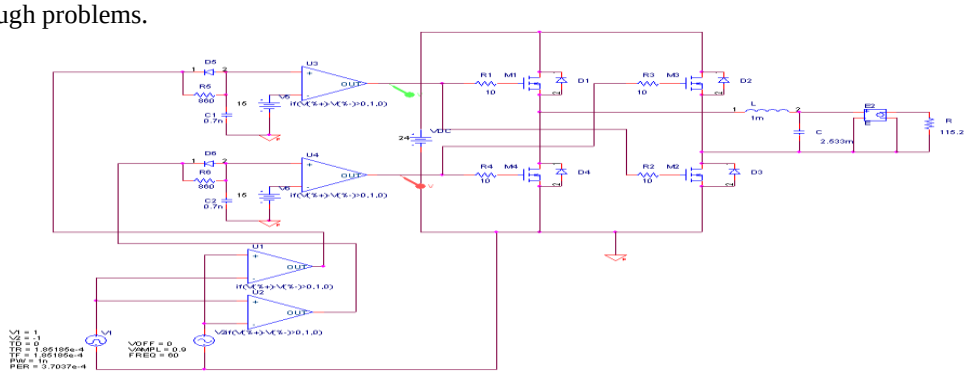

Fig.10 Modified PMW Inverter Circuit for Dead Time Insertion

Fig. (10) shows the modified inverter circuit for dead time 1μs insertion. The switching pulse is connected to R-C circuit. The output from the R-C circuit is then compared once again to get the desired switching pulse with dead time insertion. Here, the values of R and C are adjusted to get the desired 1μs.

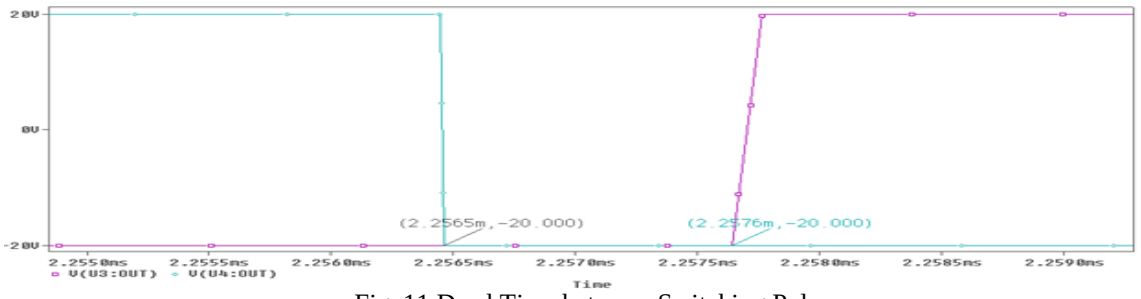

Fig. 11 Dead Time between Switching Pulse.

Fig. (11) shows the switching pulse results for both set of MOSFET switch (M1, M2 and M3, M4). From the result, the dead time is equal to 2.2576ms-2.2565ms = 1.1μs ≈ 1μs.

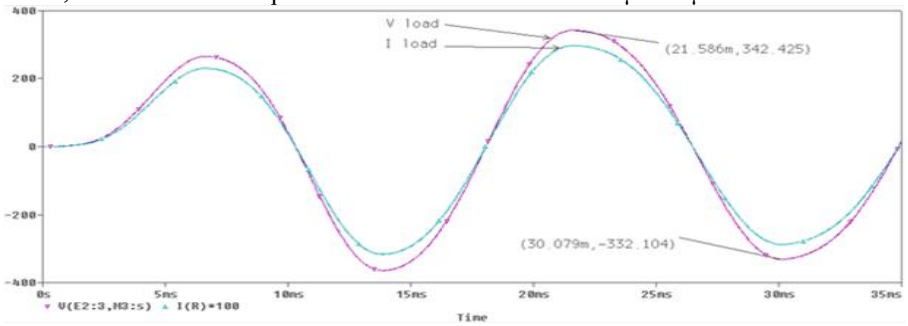

Fig.12Voltage and Current Output at the Load

Fig. (12) shows the voltage and current waveform at the output of the inverter. The output current has been multiplied by 100 for better seen. Due to the convergence problem, the transient simulation only can be running until 35ms which here, we can see that the voltage and current waveform is getting to stabilize and they are in phase.

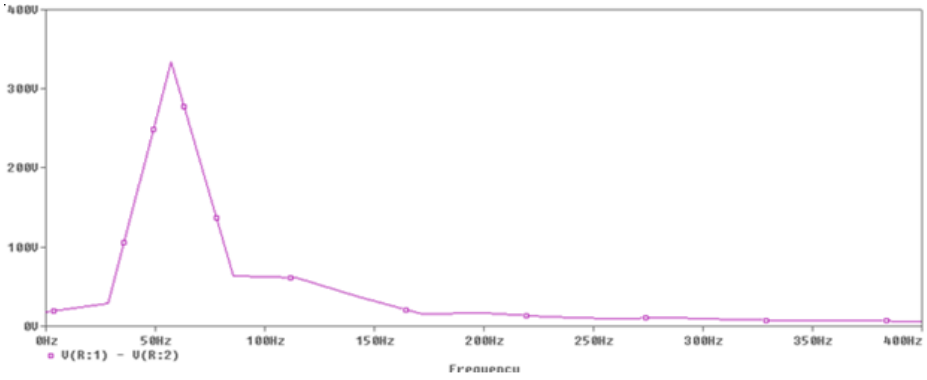

Fig. 13 Fourier series of the Output Voltage without Dead Time Insertion.

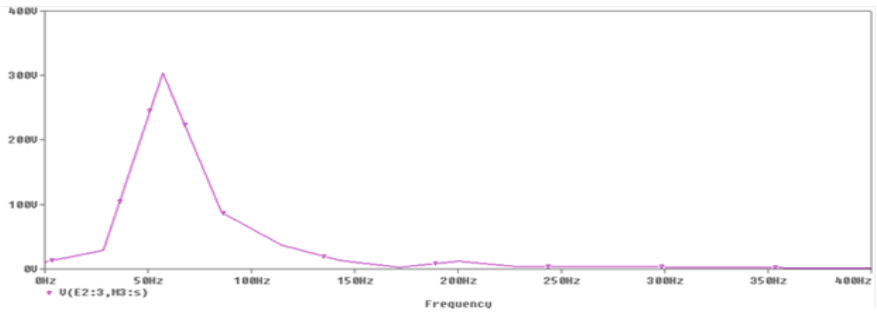

Fig. 14 Fourier series of the output voltage with dead time insertion.

Fig. (13 & 14) shows the harmonic contents of the output voltage with and without dead time insertion respectively. Form both figures; the first dominant harmonic is not present anymore because of the filter insertion at the output of inverter. Although it is a bit difficult to compare between both figures due to both figures having very low harmonic contents, it still can be seen that Fourier waveform of output voltage with dead time insertion has a slightly better result than the output voltage without dead time insertion.

VI. CONCLUSION

In this paper describes the principle of sampling PWM is based on the comparison real time of sine wave waveform (reference waveform) with a triangular carrier waveform. A high frequency triangular carrier waveform Vc is compared with a sinusoidal reference waveform Vr of the desired frequency. The PWM signal is high when the magnitude of the sinusoidal wave is higher than the triangular wave otherwise it is low. The results were proved that the inverter could produce voltage and current waveform purely. And the output voltage for PWM with dead time insertion, it has a lightly better result in term of harmonic contents although when compared with output voltage for PWM without dead time insertion, both waveforms have very low harmonic contents. Thus, the output waveform of a PWM inverter is generally improved by using a high ratio between the carrier frequency and the output fundamental frequency.

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