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Single-Phase Nine-Level Inverter with Novel Pulse Width Modulation Scheme for Resistive-Inductive Load

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Abstract: *A single-phase nine-level inverter with a novel pulse width modulation (PWM) scheme for R-L load is presented in this paper. Four triangular carrier signals that are identical to each other with an offset that is equivalent to the amplitude of the sinusoidal reference signal were used to generate the PWM signals. The inverter is capable of producing nine levels of output-voltage levels (Vdc, Vdc/4, Vdc/2, 3Vdc/4, 0,−Vdc,−Vdc/4,−Vdc/2, 3Vdc/4) from the dc supply voltage. In this paper the dc supply is obtained from ac supply which is boosted to a higher amplitude of dc voltage using dc to dc converter. In this paper, Matlab/ Simulink software is used for the system simulation. Hence, the output load voltage, current and FFT plots are obtained. This paper is focused on minimizing the number of semiconductors devices, weights, and costs for a higher number of output voltage levels.*

Index Terms: *Boost converter, modulation index, multilevel inverter, pulse width-modulation (PWM), total harmonic distortion (THD).*

I. INTRODUCTION

The Demand for renewable energy consumption has increased significantly over the years because of shortage of fossil fuels, greenhouse effect and the need to reduce pollution of our environments. Among other definitions of renewable energy include any type of energy generated from natural resources that is infinite or constantly renewed. Examples of renewable energy include solar, wind, and hydro-power. Renewable energy, due to its free availability and its clean and renewable character, ranks as the most promising renewable energy resources such asSolar energy, Wind energy that could play a key role in solving the worldwide energy crisis. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to advancement in power electronics techniques [1]. In this paper, the dc source is obtained from rectified ac voltage source with uncontrolled single phase rectifier circuit configuration. Consequently, the rectified dc voltage is stepped up using boost dc to dc converter circuit. The stepped up dc voltage is fed to a Hybrid multilevel inverter topology.

Uncontrolled rectifier circuits are of different topologies both in single and multiple phasewith different load configurations. Among them include:

1) Half-wave uncontrolled
2) Full bridge uncontrolled
   I) Mid-point configuration
   II) Full bridge configuration

Six major types of dc to dc converters have been investigated [2]. The Boost dc to dc converter otherwise called step-up converter has a dc voltage gain greater than or equal to the input voltage. The operation is in two different modes namely i) continuous current conduction and ii) discontinuous current conduction. In this paper, the selection of circuit elements were made so that the circuit operates in continuous current conduction mode. At this juncture, the Hybrid inverter topology is connected and the first member of this group is three level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment [3]–[5].Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [6].

In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three level PWM inverters. They offer improved output waveforms, smaller filter size and lower EMI, lower Total Harmonic Distortion (THD).

The three common topologies for multilevel inverters are as follows [7]:
1) Diode clamped (neutral clamped)
2) Capacitor clamped (flying capacitors)
3) Cascaded H-bridge inverter

This paper recounts the development of a novel H-bridge single-phase multilevel inverter that has three diode embedded bidirectional switches and a novel pulse width modulated (PWM) scheme.

This paper is structured as: In section I, the concept of multilevel inverter and basic types are enumerated. Section II presents the proposed H-bridge single-phase nine level inverter and its modes of operation. Section III details how the pulse width modulated (PWM) signals are generated. Here in section IV presents in details the Matlab/Simulink simulation results. In section V conclusion is presented.

II. PROPOSED MULTILEVEL INVERTER CONFIGURATION

The proposed single-phase nine-level inverter was developed from the five-level inverter in [8] – [12]. It comprises a single-phase conventional H-bridge inverter, three bidirectional switches, and a capacitor voltage divider formed by C_1, C_2, C_3, and C_4, as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, that is, less power switches, power diodes, and less capacitors for inverters of the same number of levels [3].

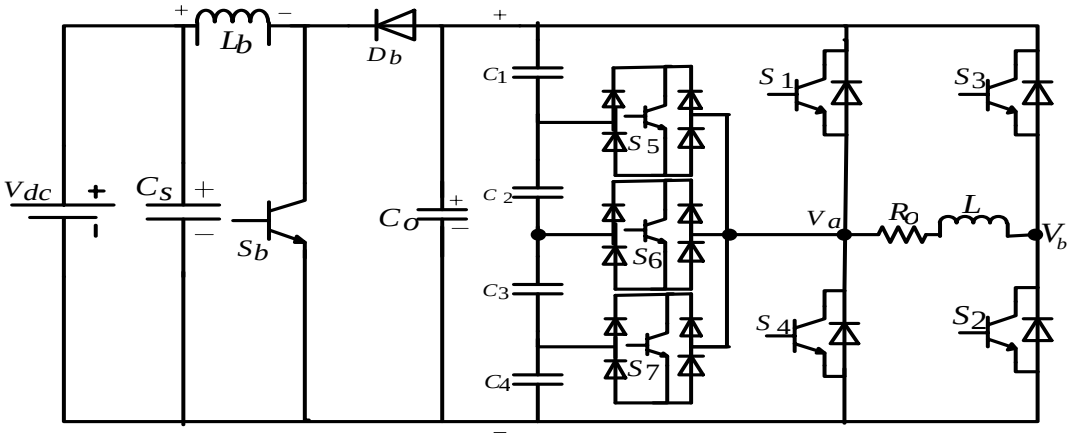

Fig. 1 Proposed single-phase nine-level with R-L load.

A single-phase fully uncontrolled rectifier with a low amplitude was connected to a Boost dc to dc converter with a high duty cycle. The inverter with R-L load was connected to the output voltage of the Boost dc to dc converter which amplifies the inverter input voltage. Proper switching of the inverter can produce nine output voltage levels (Vdc, Vdc/4, Vdc/2, 3Vdc/4, 0, −Vdc, −Vdc/4, −Vdc/2, 3Vdc/4) from the dc supply voltage.

The proposed inverter's operation can be divided into ten switching states, as shown in Fig. 2(a) – (j). The required nine-level of the output voltage were generated as follows.

1) Zero output: This level can be produced by two switching combinations; switches S_2 and S_4 are ON and all other controlled switches are OFF; terminal voltage V_{ab} is short circuited thus the output voltage becomes zero. This action is made possible because V_a and V_b are both connected to zero potential. Fig. 2(a) shows load connection at this stage. Mathematically,
$$V_{ab} = 0 = L\frac{dI_0}{dt} + I_0R_0 \quad (1)$$
2) One-fourth positive output (Vdc/4): The bidirectional switch S_7 is turned ON connecting the load positive terminal, and S_2 ON connecting the load negative terminal to the ground. All other controlled switches are turned OFF. From Fig. 2(b) the applied potential to load is Vdc/4. The mathematical expression is given by equation (2) below.
$$V_{ab} = \frac{V_{dc}}{4} = L\frac{dI_0}{dt} + I_0R_0 \quad (2)$$

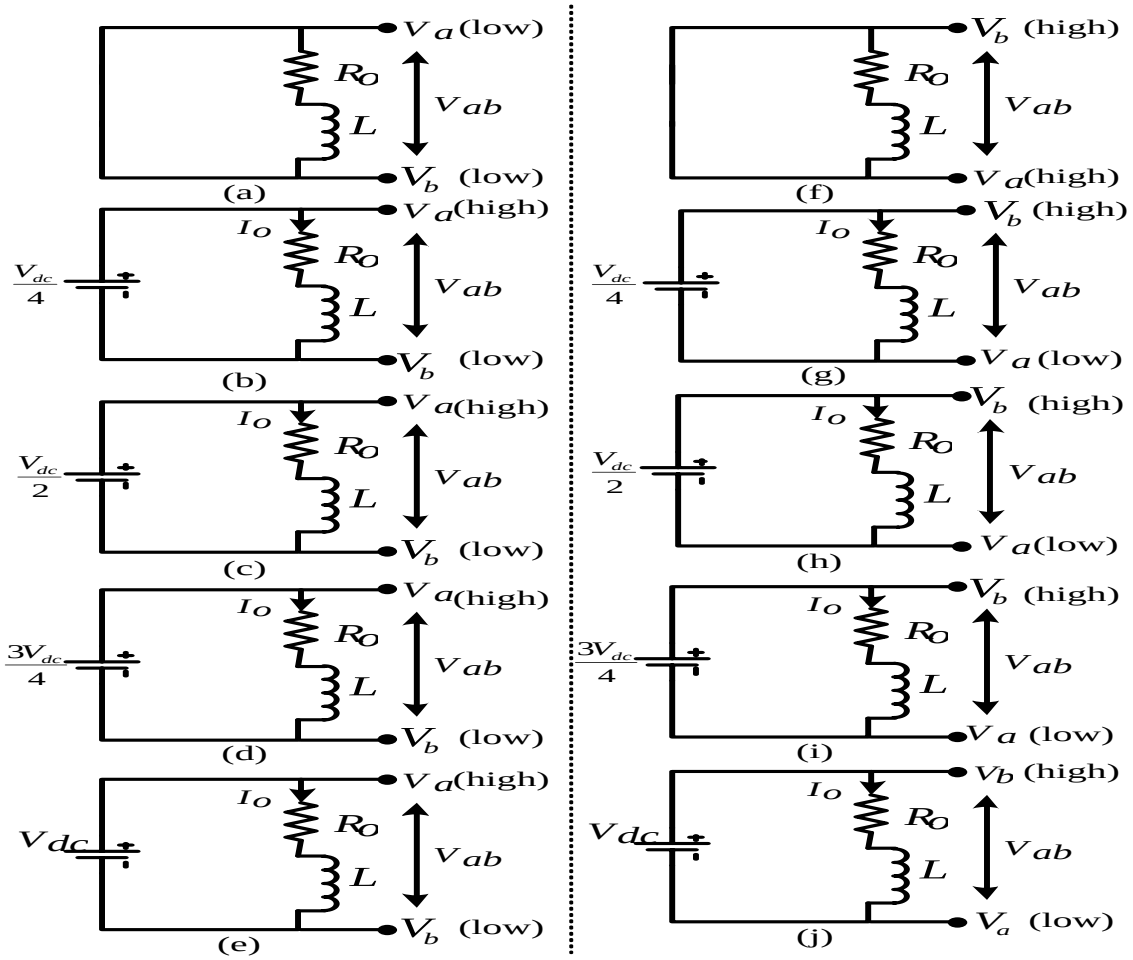

Fig. 2 Output voltage (V_{ab}) under different switching period.

3) One-half positive output(Vdc/2): The bidirectional switch $S_6$is turned ON connecting the load positive terminal, and S_2ON connecting the load negative terminal to the ground. All other controlled switches are turned OFF. From Fig. 2(c) the applied potential to load is Vdc/2. The mathematical expression is given by equation (3) below.

$$V_{ab} = \frac{V_{dc}}{2} = L\frac{dI_0}{dt} + I_0R_0 \quad (3)$$

4) Three-fourth positive output (3Vdc/4): The bidirectional switch $S_5$is turned ON connecting the load positive terminal, and S_2ON connecting the load negative terminal to the ground. All other controlled switches are turned OFF. From Fig. 2(d) the applied potential to load is Vdc/2. The mathematical expression is given by equation (4) below.

$$V_{ab} = \frac{3V_{dc}}{4} = L\frac{dI_0}{dt} + I_0R_0 \quad (4)$$

5) Maximum positive output (V_{dc}): $S_1$is ON, connecting the load positive terminal to V_{dc}, and $S_2$is ON, connecting the load terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc} as shown in Fig. 2(e). The mathematical expression is given by

$$V_{ab} = V_{dc} = L\frac{dI_0}{dt} + I_0R_0 \quad (5)$$

6) Zero output: This level can be produced by two switching combinations; switches $S_1$and S_3 are ON and all other controlled switches are OFF; terminal voltage $V_{ab}$is short circuited thus the output voltage becomes zero. This action is made possible because $V_a$and V_b are both connected to maximum potential V_{dc}. Fig. 2(f) shows load connection at this stage. Mathematically,

$$V_{ab} = 0 = L\frac{dI_0}{dt} + I_0R_0 \quad (6)$$

7) One-fourth negative output (-Vdc/4): The bidirectional switch $S_5$is turned ON connecting the load positive terminal, and S_3ON connecting the load negative terminal toV_{dc}. All other controlled switches are turned OFF. From Fig. 2(g) the applied potential to load is -V_{dc}/4. The mathematical expression is given by equation (7) below.

$$V_{ba} = -V_{ab} = \frac{-V_{dc}}{4} = L\frac{dI_0}{dt} + I_0R_0 \quad (7)$$

8) One-half negative output (-Vdc/2): The bidirectional switch $S_6$is turned ON connecting the load positive terminal, and S_3ON connecting the load negative terminal to V_{dc}. All other controlled switches are turned OFF. From Fig. 2(h) the applied potential to load is -V_{dc}/2. The mathematical expression is given by equation (8) below.

$$V_{ba} = -V_{ab} = \frac{-V_{dc}}{2} = L\frac{dI_0}{dt} + I_0R_0 \quad (8)$$

9) Three-fourth negative output (-3Vdc/4): The bidirectional switch $S_7$is turned ON connecting the load positive terminal, and S_3ON connecting the load negative terminal to V_{dc}. All other controlled switches are turned OFF. From Fig. 2(i) the applied potential to load is -3V_{dc}/4. The mathematical expression is given by equation (9) below.

$$V_{ba} = -V_{ab} = \frac{-3V_{dc}}{4} = L\frac{dI_0}{dt} + I_0R_0 \quad (9)$$

Table 1:OUTPUT VOLTAGE ACCORDING TO THE SWITCHES' (OFF) 0 – (ON) 1 CONDITION

States	S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_a	V_b	V_{ab}
1	0	1	0	1	0	0	0	0	0	0
2	0	1	0	0	1	0	0	$\frac{V_{dc}}{4}$	0	$\frac{V_{dc}}{4}$
3	0	1	0	0	0	1	0	$\frac{V_{dc}}{2}$	0	$\frac{V_{dc}}{2}$
4	0	1	0	0	0	0	1	$\frac{3V_{dc}}{4}$	0	$\frac{3V_{dc}}{4}$
5	1	1	0	0	0	0	0	V_{dc}	0	V_{dc}
6	1	0	1	0	0	0	0	V_{dc}	V_{dc}	0
7	0	0	1	0	1	0	0	0	$\frac{V_{dc}}{4}$	$\frac{-V_{dc}}{4}$
8	0	0	1	0	0	1	0	0	$\frac{V_{dc}}{2}$	$\frac{-V_{dc}}{2}$
9	0	0	1	0	0	0	1	0	$\frac{3V_{dc}}{4}$	$\frac{-3V_{dc}}{4}$
10	0	0	1	1	0	0	0	0	V_{dc}	$-V_{dc}$

10) Maximum negative output (-Vdc): The bidirectional switch $S_4$is turned ON connecting the load positive terminal, and S_3ON connecting the load negative terminal toV_{dc}. All other controlled switches are turned OFF. From Fig. 2(j) the applied potential to load is -V_{dc}. The mathematical expression is given by equation (10) below.

$$V_{ba} = -V_{ab} = -V_{dc} = L\frac{dI_0}{dt} + I_0R_0 \quad (10)$$

Table I shows the switching combinations that generated the nine output voltage levels (Vdc, Vdc/4, Vdc/2, 3Vdc/4, 0, −Vdc, −Vdc/4, −Vdc/2, 3Vdc/4).

III. PWM MODULATION

A novel PWM modulation strategy was introduced to generate the PWM switching signals. Four carrier signals ($V_{carrier\ 1}$,$V_{carrier\ 2}$,$V_{carrier\ 3}$,and $V_{carrier\ 4}$) were compared with a control signal ($V_{control}$,) in Fig. 5. The carrier signals had the same frequency and amplitude and were in phase with offset value that was equivalent to its amplitude. The carrier signals were each compared with control signal.

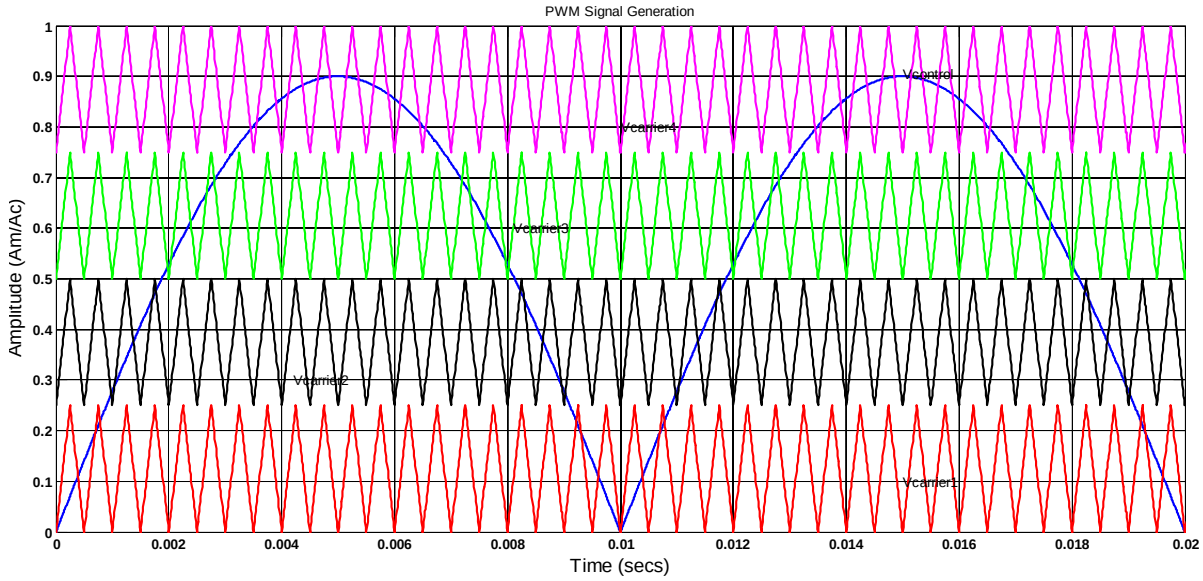

Fig. 5 PWM switching generation.

The general structure of the proposed system is given in given Fig. 6. In this modulation strategy, the fundamental frequency PWM (A) is a square wave signal synchronized with the modulation waveform; A=1 during the positive half cycle of the modulation signal, and A=0 during negative half cycle. Carrier based pulse width modulation (CBPWM) is based on comparison of rectified sinusoidal reference signal, with carrier to determine the voltage level that the inverter should switch to. The base PWM signals (A, B, C, D, E) for hybrid PWM controller are shown in Fig. 7. The hybrid PWM controller is implemented using a simple combinational logic, hence, it can be processed very quickly with less number of logic components.

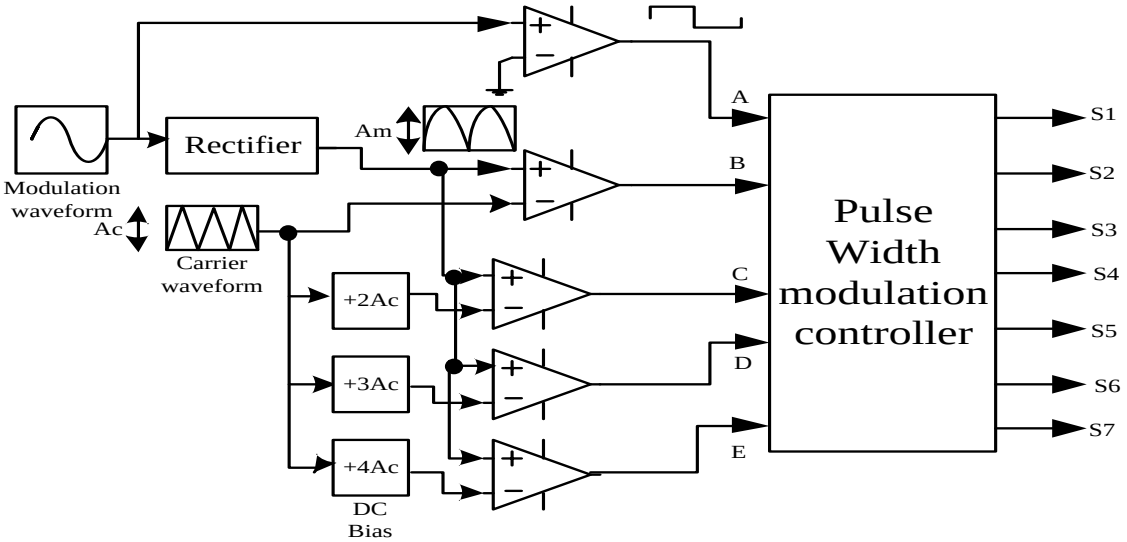

Fig. 6 Scheme of Pulse Width Modulation generator.

The functions of the combinational logic for a nine level hybrid PWM are expressed as

S1=AE+$A\bar{B}$; S2=A; S3=$\bar{A}$; S4=A$\bar{B}$+$\bar{A}E$;

S5=AD$\bar{E}$+$\bar{A}B\bar{C}$; S6=C$\bar{D}$; S7=AB$\bar{C}$ + $\bar{A}D\bar{E}$. (11)

The generated signals are displayed in Fig. 8. It is shown that each gate signal is composed of both high and low switching frequency signals per cycle. In the full cycle plot it is observed that the switching signal ofS_1,S_4,S_5, S_6, and S_7 are operated at a high frequency while S_2 and S_3 are operated at fundamental frequency.

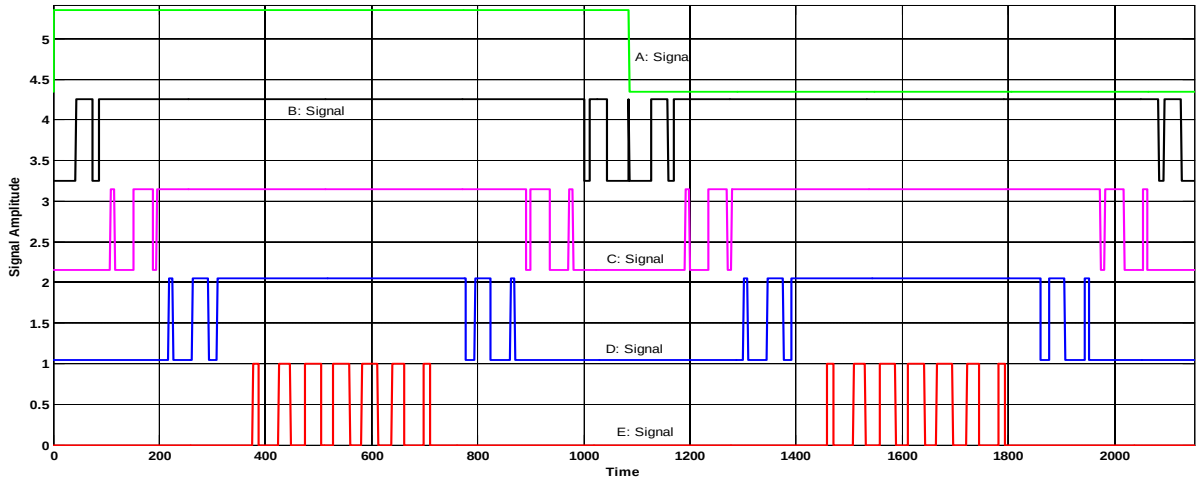

Fig. 7. Base PWM signals for nine-level inverter circuit configuration.

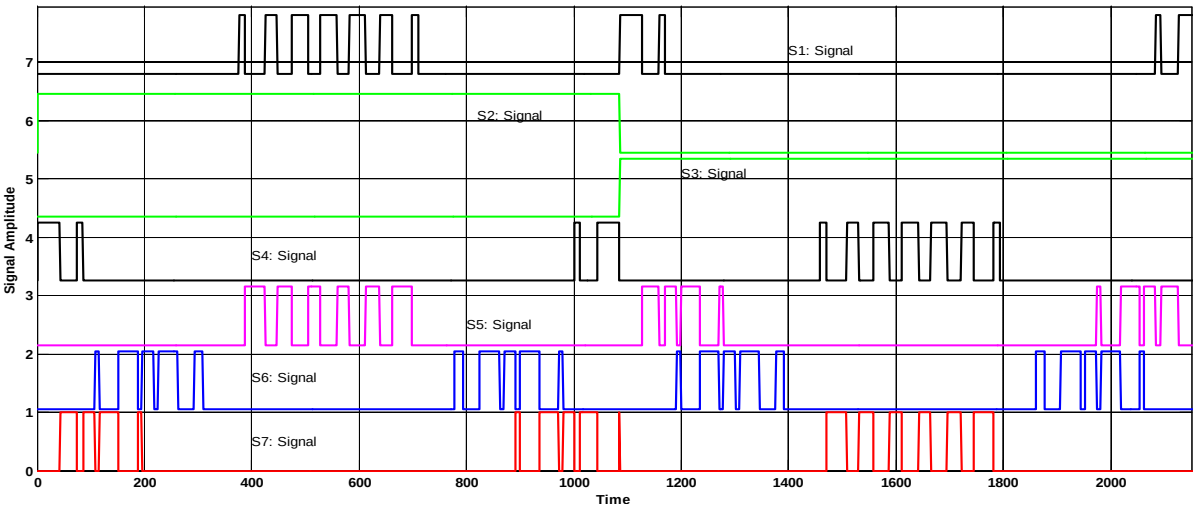

Fig. 8 Switching pattern for the single-phase nine-level inverter

For one cycle of the fundamental frequency, the proposed inverter operated through eight modes. Fig.9 shows the per unit output-voltage signal for one cycle. The eight modes are described as follows:

$$\left.\begin{array}{c} Mode\ 1: 0 < \omega t < \theta_1\ and\ \theta_6 < \omega t < \pi \\ Mode\ 2: \theta_1 < \omega t < \theta_2\ and\ \theta_5 < \omega t < \theta_6 \\ Mode\ 3: \theta_2 < \omega t < \theta_3\ and\ \theta_4 < \omega t < \theta_5 \\ Mode\ 4: \theta_3 < \omega t < \theta_4 \\ Mode\ 5: \pi < \omega t < \theta_7\ and\ \theta_{12} < \omega t < 2\pi \\ Mode\ 6: \theta_7 < \omega t < \theta_8\ and\ \theta_{11} < \omega t < \theta_{12} \\ Mode\ 7: \theta_8 < \omega t < \theta_9\ and\ \theta_{10} < \omega t < \theta_{11} \\ Mode\ 8: \theta_9 < \omega t < \theta_{10} \end{array}\right\} \quad (12)$$

The phase angle depends on modulation index M_a. Theoretically, for a single control (reference) signal and a single carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{A_c} \quad (13)$$

While for a single-control signal and a dual carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{2A_c} \quad (14)$$

Thus, for a single-control signal and a triple carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{3A_c} \quad (15)$$

Since the proposed nine-level PWM inverter utilizes four carrier signals, the modulation index is defined to be

$$M_a = \frac{A_m}{4A_c} \quad (16)$$

Where A_c is the peak to peak value of the carrier signal and A_m is the peak to peak value of the voltage reference signal.

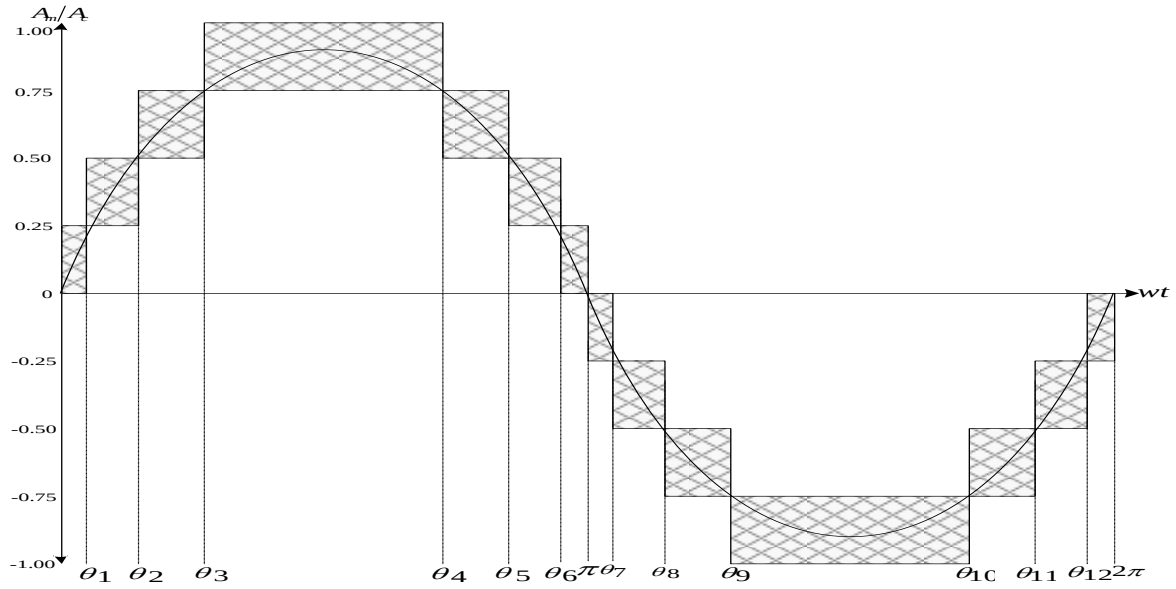

Fig. 9 Nine-level output (V_{ab}) and switching angles.

IV. SIMULATION RESULTS

The single-phase nine-level inverter topology for the proposed modulation strategy uses single reference/control signal and four carrier signals which was modeled and simulated in MATLAB and is shown below. The simulation was carried out with two input signals namely sine and triangular waves with differentamplitudes and frequencies. Seven firing signals were generated as shown in Fig. 10 below.

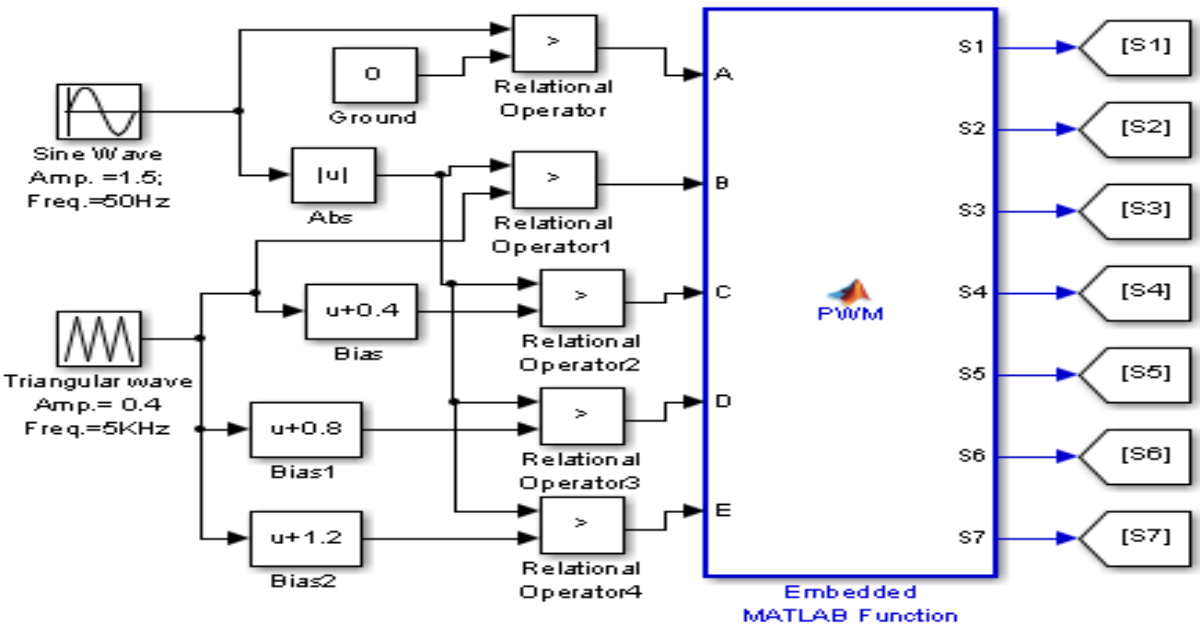

Fig. 10Matlab/Simulink model of firing signals.

Fig. 10 consists of a sine wave generator, triangular wave, rectifier circuit, four offset generator, five comparators, many logic gates (OR, AND, etc.). The logic gates are embedded in Simulink subsystem as shown in the figure above. The signals are generated from the expressions in equation (11).

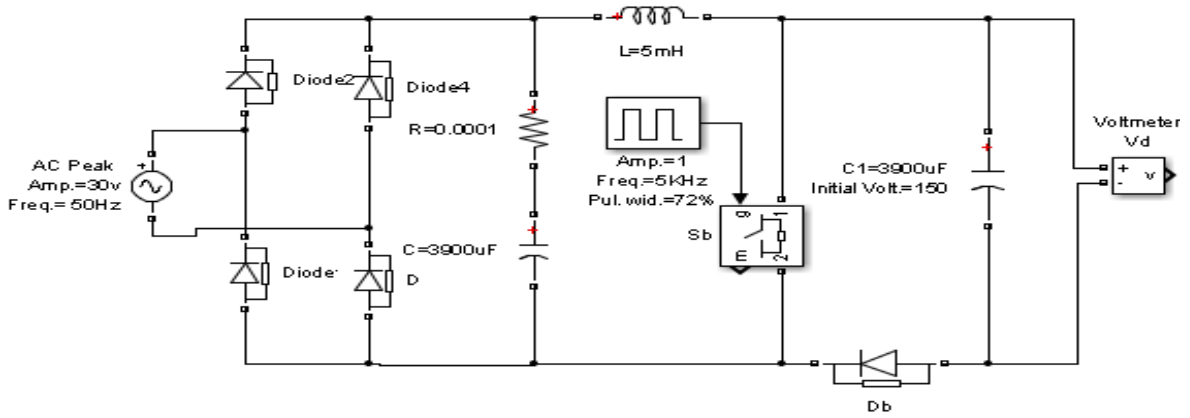

Fig. 11Matlab/Simulink model of AC to DC converter.

Fig. 11 shows Matlab/Simulink model of AC to DC circuit converter. This model is composed ofuncontrolled full wave rectifier circuit with low AC input voltage. The output voltage is filtered with a capacitor value of 3900µF by 100V. This output rectifier voltage is supplied to a Boost DC to DC converter which aids in enhancing the input voltage to the inverter circuit to higher amplitude.

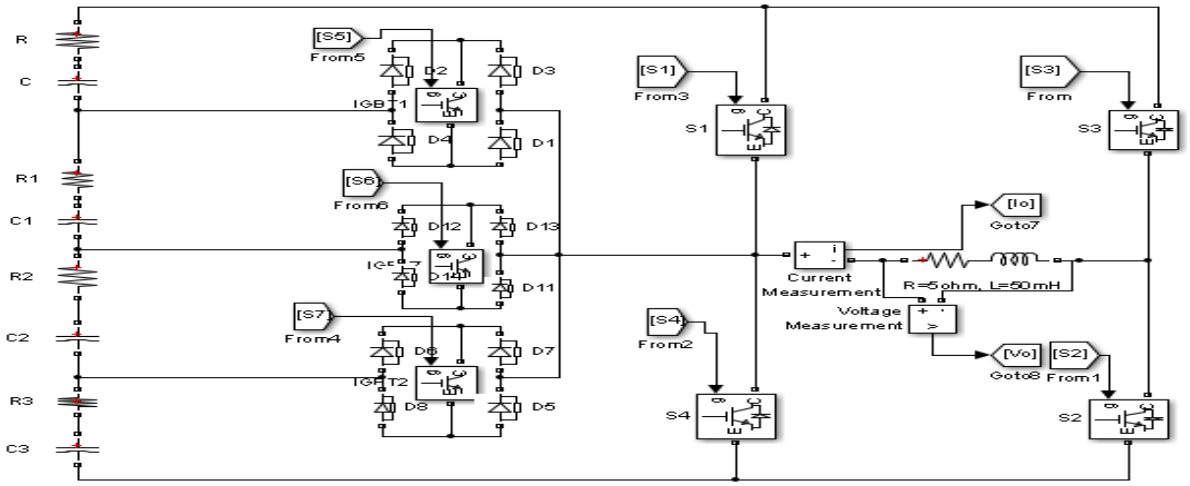

Fig. 12Proposed single-phase nine-level inverter configuration

Fig. 12 shows Matlab/Simulink model for proposed single-phase nine-level inverter topology with resistive-inductive load.The inverter input voltage is connected from Fig. 11 above also, the firing signals are sourced from Fig. 10.

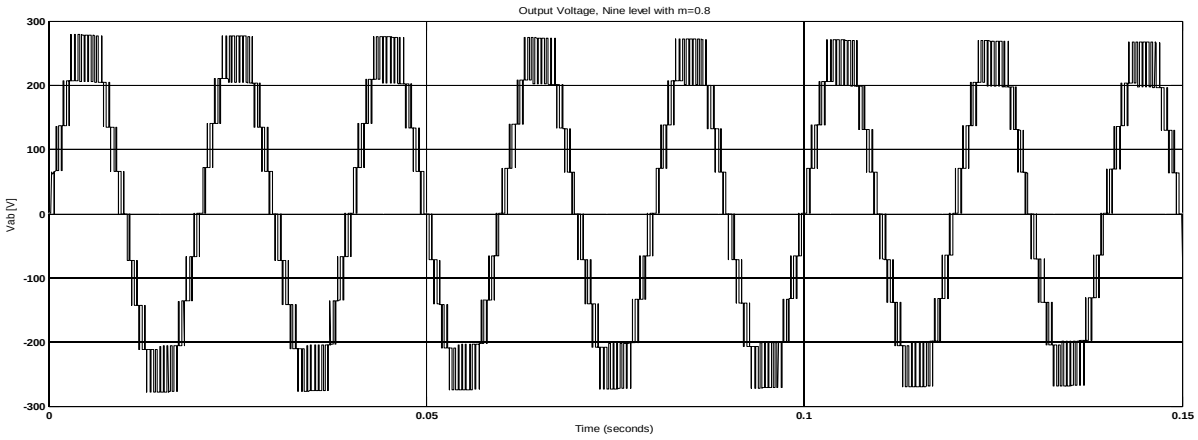

Fig. 13 Inverter Output Voltage

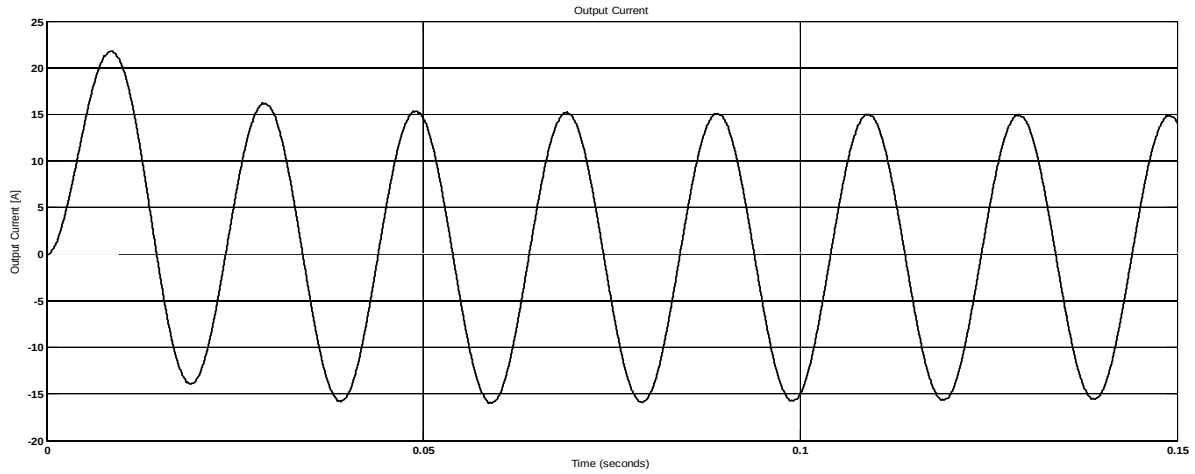

Fig. 14 Inverter Output Current

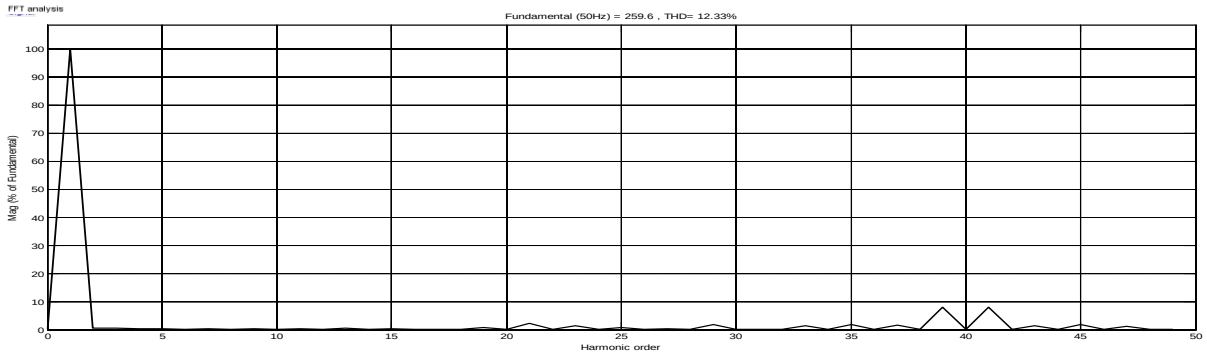

Fig. 15 Output FFT analysis

Fig. 13 shows seven and half cycles of the inverter output voltage of approximately 260VAC at a modulation index of 0.8 under an R-L load. Fig. 14 depicts the inverter output current of a value 15A which lags the output voltage by $72°.34'$ load angle. Thus, the load impedance is approximately 16.48Ω. Fig. 15 shows the FFT spectrum of the output voltage of the nine-level inverter with THD of 12.33%.

V. CONCLUSION

This paper has presented a single-phase nine-level inverter with reduced number of switches. A sine wave reference signal andmultiple carrier triangular signalspulse width modulation method have been proposed. The behaviour of the proposed multilevel inverter was analysed in detail. It is found that this method of modulation scheme gives a reduced number of circuit control components when compared to the same output voltage levelof diode clamped topology. As a result of that, the circuit configuration can be realised with low cost and less weight. Furthermore, it gives a better quality output voltage and THD value. Therefore, theproposed multilevel inverter is recommended for photovoltaic applications.

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