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Effect of Gate Length on the DC and RF Performance of GaN HEMT Devices

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ABSTRACT: *In this work, we report GaN high-electron-mobility-transistors (HEMTs) on SiC with gate lengths of various dimensions for optimum performance. 125 µm gate width, 4 µm drain source spacing AlGaN/GaN HEMTs with gate lengths of 0.3, 0.6, 0.8, and 1.0 µm were fabricated. For devices with the gate lengths in the range of 0.3-0.8 µm, with an increase in gate length, the output power density (P_{out}) at 4 GHz is increased from 1W/mm to 1.5W/mm, although the $I_{ds,max}$, g_m, f_t and f_{max} values are decreased in acceptable limits. The great enhancement in P_{out} with the increase in the gate length is due to fact that the increase in gate length affects the controllability of the electric field under the channel; hence the peak value of the electric field under gate contact decreases and the electric field variation under the gate contacts is smoother. For the device with the gate length of 1.0 µm $I_{ds,max}$, g_m values are almost the same as the values with the gate length of 0.8 µm, but P_{out} is decreased, since with this gate length the increase in parasitic capacitances is more effective and this limits the improvement due to the gate length increase.*

Keywords *-GaN HEMT, Gate length, RF power applications, coplanar waveguide, and power amplifiers.*

I. INTRODUCTION

AlGaN/GaN high-electron-mobility-transistor (HEMT) devices are of great interest for high power, high frequency, high temperature and low noise radio frequency (RF) applications due to their high breakdown electric field, high breakdown voltage, high saturation velocity and high thermal conductivity[1-3]. In addition, AlGaN/GaN HEMTs include high conduction band offset and high piezoelectricity resulting in high current density and high power density compared to GaAs and InP based HEMTs[4,5].

In this work, a systematic study of the effect of the gate length on small signal gain, output power, efficiency and cut off frequency is presented. GaN-HEMTs are fabricated with different gate lengths. Increasing the gate length helps control the electric field under the channel that is caused by gate contact. Thus, it decreases the peak electric field value and the electric field distribution is smoothened under the gate contact, resulting in the improvement of the breakdown voltage and the output power performance of the HEMT. The benefit is due to the reduced high-field trapping effect resulting in the prevention of electron emission and electron trapping. As a result, the increase of the gate length helps the reduction of the current collapse effect of the HEMTs. In addition to output power performance, increasing the gate length also has an impact on the noise performance of HEMTs.

The schematic and layout of the designed HEMT is given in Fig. 1 and in Fig. 2. In Fig. 1, L_{gs} is 0.6 µm and four different gate lengths are designed as 0.3, 0.6, 0.8 and 1.0 µm. The thickness of the Si_3N_4 dielectric passivation layer is 300 nm. The measured HEMT devices have six fingers and the average gate-to-gate distance is 60 µm (Fig. 2).

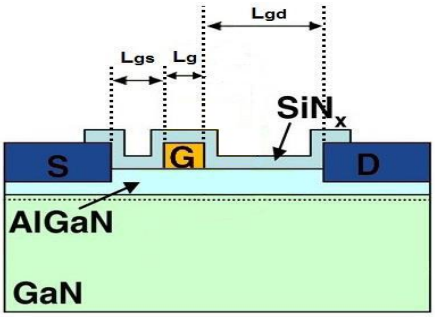

Fig.1. Schematic of an AlGaN/GaN HEMT structure.

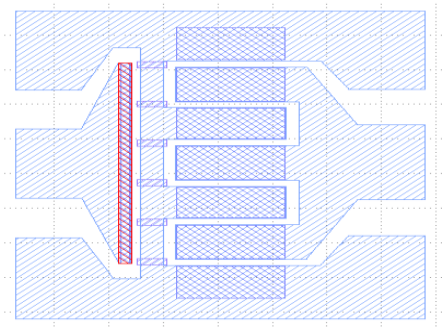

Fig. 2. Layout of an AlGaN/GaN HEMT structure.

II. DEVICE REALIZATION

An AlGaN/GaN HEMT epitaxial structure was grown on a semi-insulating SiC substrate by metal organic chemical vapor deposition[6-8]. The epilayer consists of a 15 nm AlN nucleation layer, 2 µm undoped GaN buffer layer, approximately 1.5 nm AlN interlayer, 20 nm undoped $Al_{0,22}Ga_{0,78}N$ layer and a 2 nm GaN cap layer on the top of the structure. The Hall mobility was 1384 $cm^2V^{-1}s^{-1}$ whereas the sheet carrier concentration was 1.51×10^{13} cm^{-2}.

The fabrication process flow diagram of the HEMTs is shown in Fig. 3[9-12].

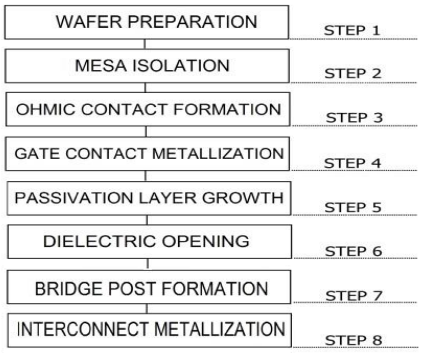

Fig. 3. Flow chart of the GaN HEMT fabrication process.

Mesa etching was performed with ICP-RIE with a $Cl_2/BCl_3/Ar$ gas mixture. Ohmic contacts were formed by evaporated Ti/Al/Ni/Au (12 nm/120 nm/35 nm/65 nm) metals by the e-beam evaporation method and annealing them in nitrogen ambient at 850 °C for 30 s. Ohmic contact resistance was 0.12 Ω-mm and the sheet resistance was 508 $\Omega\text{-}\square^{-1}$ measured by using the transfer length measurement (TLM) patterns. Ni/Au (50 nm/300 nm) was deposited for gate contacts. The devices were passivated with a 300 nm-thick Si_3N_4 layer grown by plasma-enhanced chemical vapor deposition. After the passivation, the openings, where the interconnect metal will be deposited on, were formed by means of the dry etching of ICP-RIE with CHF_3 gas. The airbridge post structures were constituted for preventing any case of the short circuit of the metals by functioning as a jumper. Finally, a relatively thick Ti/Au metal stack with e-beam evaporation was deposited as an interconnection on the sample, and then the fabrication process was completed with this last step. Figure 4 shows a 6×125 µm wide device's optical microscope image and Figure 5 shows the SEM images of the gates with L_g= 0.3, 0.6, 0.8, and 1.0 µm.

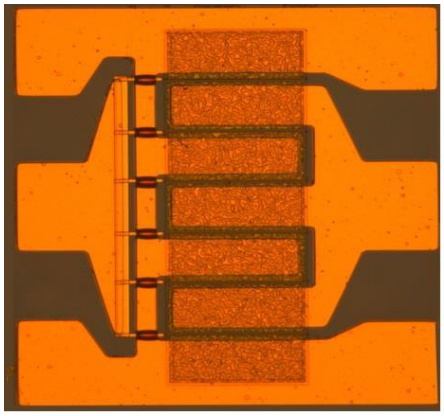

Fig. 4 Optical microscope image of fabricated 6×125μm HEMT.

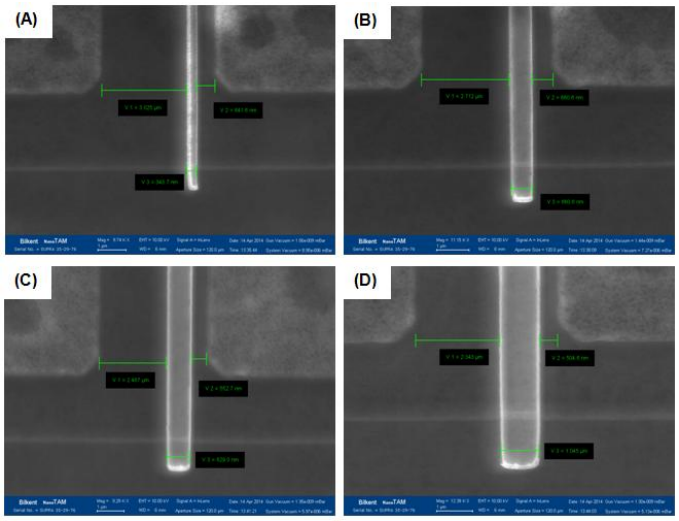

Fig. 5. SEM images of gates with an (A) 0.3 μm, (B) 0.6 μm, (C) 0.8 μm, (D) 1.0 μm gate length (L_g).

III. RESULTS AND DISCUSSIONS

DC on wafer measurements were performed using an Agilent B1500A semiconductor device parameter analyzer. For DC IV characterization, the gates were biased from -6V to 1V in a step of 1 V, and the drain current-voltage (I_{ds}–V_{ds}) characteristics were measured for a 6×125 μm AlGaN/GaN HEMT with L_g = 0.3, 0.6, 0.8, and 1.0 μm (Fig. 6). It can easily be seen that all of the devices have good pinch off characteristics and the devices completely pinch off at V_{gs}= -5V.

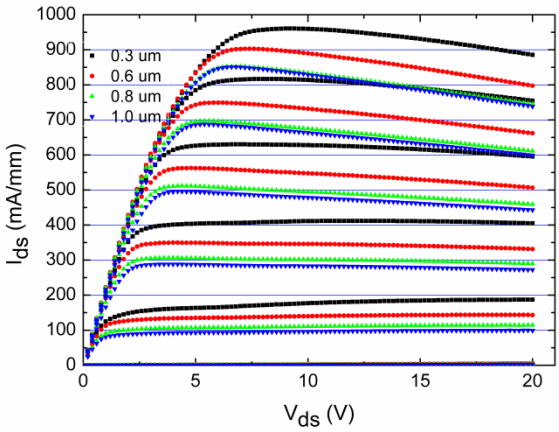

Fig. 6. Drain current-voltage (I_{ds}–V_{ds}) characteristics of a 6×125 μm AlGaN/GaN HEMT with L_g = 0.3, 0.6, 0.8, and 1.0 μm. The gate bias was swept from +1V to -6 V in a step of -1 V.

The extrinsic transconductance (g_m) for all the devices was also measured. Fig. 7 shows the transconductance (g_m–V_{ds}) characteristics of 6×125 µm AlGaN/GaN HEMT with L_g = 0.3, 0.6, 0.8, and 1.0 µm. It is seen that the maximum value of g_m is above 250 mS/mm for all the devices.

The change in the $I_{ds,\ max}$ and g_m values as a function of the gate length is given in Figs. 8 and 9, respectively. As can be seen in Figs. 8 and 9, $I_{ds,\ max}$ and g_m are decreased with the increase in L_g from 0.3 to 0.8 µm. A maximum $I_{ds,\ max}$ of 960 mA/mm was obtained for the shortest gate length, i.e., L_g = 0.3 µm, and a minimum $I_{ds,\ max}$ of 852 mA/mm was obtained for L_g = 0.8 µm. A maximum g_m of 236 mS/mm was obtained for the shortest gate length, i.e., L_g = 0.3 µm, and a minimum g_m of 203 mS/mm was obtained for L_g = 0.8 µm. $I_{ds,\ max}$ and $g_m$were not changed with the increase of L_g from 0.8 µm to 1.0 µm. The maximum current density of 852 mA/mm and the extrinsic transconductance of 203 mS/mm was obtained for both L_g = 0.8 µm and L_g = 1.0 µm.

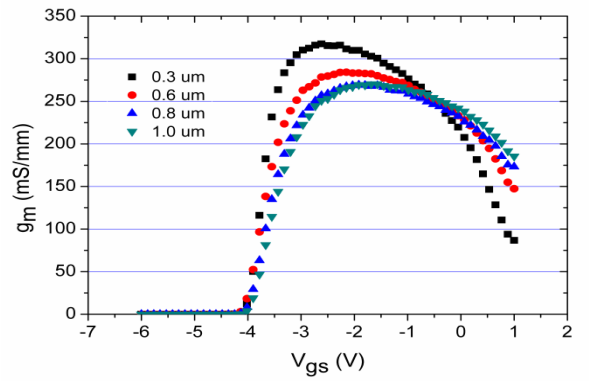

Fig. 7. Transconductance (gm–Vgs) characteristics of a 6×125 µm AlGaN/GaN HEMT with Lg = 0.3, 0.6, 0.8, and 1.0 µm. The gate bias was swept from −6 to 1 V in a step of 1 V.

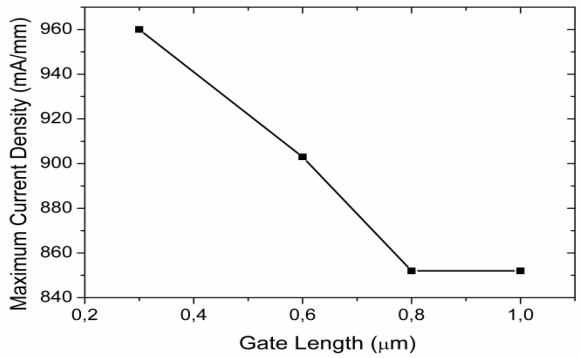

Fig. 8. The change of $I_{ds,\ max}$ as a function of the gate length.

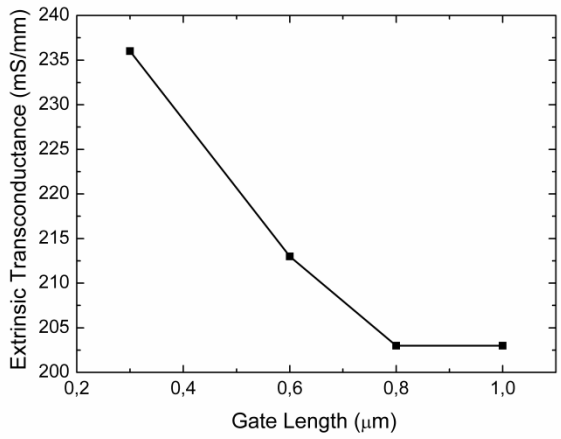

Fig. 9. The change in g_m as a function of the gate length.

According to these results, it can be said that when the gate length increases up to an optimum point, this increase helps the controllability of the electric field under the channel caused by the gate contact. Thus, it decreases the peak value of the electric field and improves the smoothness of the electric field under the gate contact. Due to this effect, the movement of electrons along the 2DEG channel is more difficult and this results in the decrease in maximum current density and the extrinsic transconductance. There is no change in the maximum current density and the extrinsic transconductance when the increase of the gate length is over the optimum point, because over the optimum gate length, the electric field under the channel caused by gate contact does not change any more.

On-wafer radio frequency (RF) measurements were carried out using a Cascade Microtech Probe and an Agilent E8361A PNA in the 1–20 GHz range. The change of the unity current gain cut off frequency, f_t and the maximum oscillation frequency, f_{max} as a function of L_g is shown in Figs. 10 and 11, respectively.

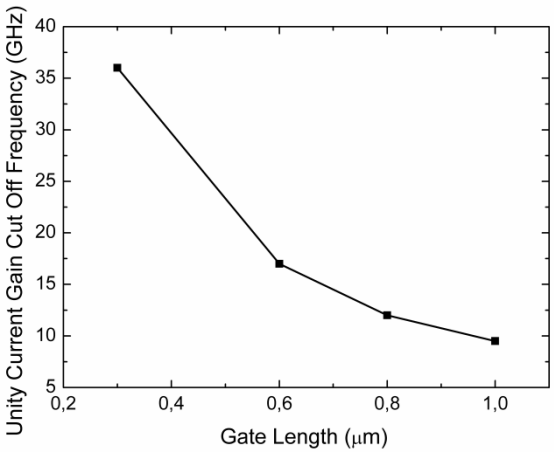

Fig. 10. The change of unity current gain cut off frequency (f_t) as a function of the gate length.

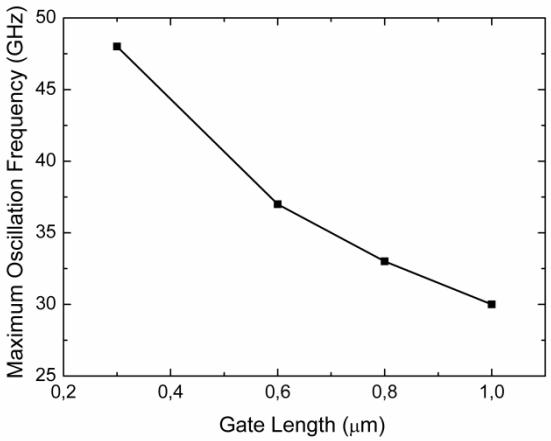

Fig. 11. The change of the maximum oscillation frequency (f_{max}) as a function of the gate length.

The unity current gain cut off frequency (f_t) and the maximum oscillation frequency (f_{max}) were decreased with the increase in L_g due to the increasing capacitive effects as expected[13,14]. A unity current gain cut off frequency (f_t) of 36 GHz and maximum oscillation frequency (f_{max}) of 48 GHz were obtained for L_g = 0.3 μm and a minimum unity current gain cut off frequency (f_t) of 9.5 GHz and maximum oscillation frequency (f_{max}) of 30 GHz were obtained for the L_g = 1.0 μm.

A large signal load pull measurement was carried out using a Maury Microwave automated load pull system at 4 GHz to obtain output power performance. The data were taken on-wafer at room temperature without any thermal management. All the HEMTs were measured at a drain bias of 30 V, and the output powers were obtained at 2dB gain compression. A summary of the output power values obtained as a function of the gate length is shown in Fig. 12. The output power was increased when L_g was increased from 0.3 to 0.8 μm. A maximum output power of 1461 mW/mm was obtained for L_g = 0.8 μm and a minimum output power density of 1012 mW/mm was obtained for L_g = 0.3 μm.

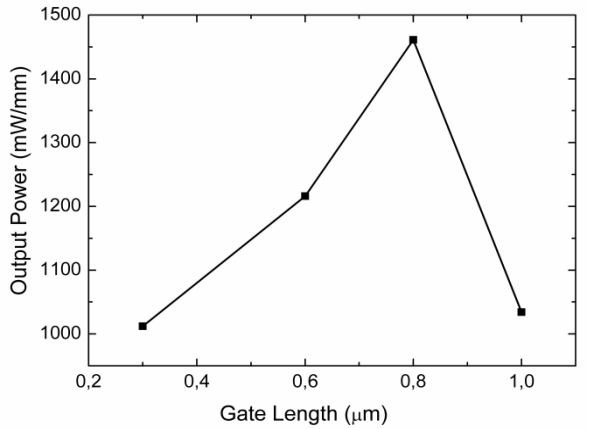

Fig. 7. Summary of output power as a function of the gate length. The devices were biased at V_{ds} = 30 V, V_{gs} = -2.9 V and 4 GHz.

The output power density of HEMTs was decreased when L_g is above 0.8 μm. Up to the optimum value of the gate length, the increase in gate length smoothens the electric field under the gate contact and decreases the electron emission and electron trapping. As a result it helps the reduction of the current collapse and increases the output power density of the HEMTs. L_g of 0.8 μm is optimum for the HEMTs with 4 μm drain-source spacing. When the gate length exceeds the optimum length, the electric field under the channel caused by gate contact does not change, but due to the decrease of L_{gd} (gate drain spacing), the increase in parasitic capacitances especially in gate drain capacitance, C_{gd}becomes effective and this limits the gain and output power performance of the HEMTs.

The DC, small signal, and large signal results are summarized in TABLE 1.

TABLE I. Summary Of The Results Of The AlGaN/GaN HEMTs with Varying Gate Length.

L_g (μm)	0.3	0.6	0.8	1.0
$g_{m,max}$(mS/mm)	236	213	203	203
$I_{ds,max}$(mA/mm)	960	903	852	852
f_t (GHz)	36	17	12	9.5
f_{max} (GHz)	48	37	33	30
Output Power (mW/mm) @2dB comp.	1012	1216	1461	1034

IV. CONCLUSION

A systematic study has been performed to investigate the effect of a gate length on the DC characteristics, small signal gain and large signal performance of GaN-channel HEMTs. For HEMTs with six fingers, 125 μm gate width, 4 μm drain-source spacing, 300 nm-thick Si_3N_4 as a dielectric passivation layer, an optimum gate length was found to be 0.8 μm for maximum RF output power performance. It was observed that the increase in the gate length from 0.3 μm to the optimum gate length, 0.8 μm, results in increase of controllability of the electric field under the channel caused by gate contact and decreases the leakage current. Thus it decreases the maximum current density and the extrinsic transconductance, but increases the RF output power density of HEMTs. When the gate length is over the optimum value of 0.8 μm, the length between drain and gate contacts decreases below 2.2 μm, the capacitive effects between the gate and drain begin to dominate and the output power density of HEMTs are decreased. In order to improve the power density performance further the drain-source spacing should be improved as a future work and then it may be possible to obtain larger gate lengths without any degradation in output power density values of HEMTs.

V. ACKNOWLEDGEMENTS

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