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Design of up/down counter based on dual mode logic and Low power Hybrid dual mode dynamic flip-flop

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ABSTRACT *– This paper introduces a 4-b Johnson up-down counter that incorporates low power dual dynamic node pulsed hybrid flip-flop (DDFF) with clock gating technology and a dual mode logic (DML) in the counter. Clock gating disable the clock signal when the input data does not change the stored data. A DML mode logic is introduced here which improves the speed performance of the design, also achieving significant energy consumption reduction. The large capacitance in precharge node is eliminated by the DDFF and DDFF-ELM designs by following a split dynamic node structure. The DDFF offers power reduction. The DDFF-ELM reduces pipeline overhead. 4-b Johnson up-down counter is used to magnify the performance improvement of the designs, to which the DML logic is introduced. An area, power, and speed efficient method is presented here that incorporates complex logic functions into the flip-flop. The DML logic used in DDFF-ELM helps to achieve low power and high speed requirements. The simulation results are compared using T-Spice*

KEYWORDS *- Low power, DDFF, high speed, DML Logic, embedded logic, counter*

I. INTRODUCTION

For VLSI designer's power consumption has become a very important issue. Sequential logic circuits, such as registers, memory elements, counters etc., are heavily used in the implementation of Very Large Scale Integrated (VLSI) circuits [7]. Power dissipation is critical for battery-operated systems, such as laptops, calculators, cell phones and MP3 players since it determines the battery life. Therefore, designs are needed that can consume less power while maintaining comparable performance. Flip-flop is a data storage element. The operation of the flip-flops is done by its clock frequency [3] [7]. When multistage Flip-Flop is operated with respect to clock frequency, it processes with high clock switching activity and then increases time latency. Therefore it affects the speed and energy performance of the circuit [3]. Various classes of flip-flops have been proposed to achieve high-speed and low-energy operation [5]. In the past decades, many works has been dedicated to improve the performance of the flip-flops. Latches and flip-flops are the basic elements for storing information. The flip-flops and latches could be grouped under the static and dynamic design styles. The former type of designs dissipates lower power and the latter type includes the modern high performance flip-flops [11][12]. Several hybrid flip-flop designs have been proposed to reduce the power and delay. Some flip-flops analyzed here are PowerPC 603 flip-flop, Semi-dynamic flip-flop (SDFF), Conditional data mapping flip-flop (CDMFF), Cross charge control flip-flop (XCFF) and Dual dynamic node hybrid flip-flop (DDFF). For a design engineer the trade-off of any of these flip-flops is very important when designing a circuit. Therefore a flip-flop which meets the designer requirements have to be developed.A new dual dynamic based flip-flop is presented in this paper which involves clock gating for further power reduction. The clock gating technique [11] has been developed to avoid unnecessary power consumptions, like the power wasted by timing components during the time when the system is idle.

The rest of this paper is divided as follows. Section II discusses the disadvantages of existing flip-flop structures and challenges in achieving high performance. In section III, the proposed architecture and its operation are provided. Section IV describes 4-b Johnson up/down counter with clock gated dual dynamic flip-flops and DML logic. Section V includes the performance analysis and simulation result comparisons. In section VI, we conclude with the improvements of the proposed designs over the existing modern high performance designs.

II. ANALYSIS OF FLIP-FLOP TOPOLOGIES

PowerPC 603 is one of the most efficient classic static structures. It is a master-slave latch. Its main advantage is low power feedback and short direct path. It is constructed by cascading two identical pass gate latches. This flip-flop is a transmission gate flip-flop. The large D-Q delay and CLK node capacitances make the design inferior in performance. The Hybrid Latch Flip-Flop (HLFF) is not the fastest but has a lower power. The Hybrid Latch Flip-Flop is a high performance flip-flop. It does not have a positive hold time but robust to clock signal slopes. For high performance designs, HLFF is the best solution. But for embedding the logic functions, HLFF is inefficient. This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This flip-flop has small delay and small area. This flip-flop falls under hybrid category with negative setup time [2][6]. Semi Dynamic Flip-Flop (SDFF) is a combination of static and dynamic circuits. They are called as hybrid structures because they consist of a dynamic frontend and a static output. It has the capability of incorporating logic very efficiently, because unlike the true single phase latch (TSPC), only one transistor is driven by the data input [3]. SDFF is the fastest classic hybrid structure. But it has large CLK load, so not efficient as far as power consumption is concerned .The flip-flop also has large pre-charge capacitance. This is still best suited for high performance designs, though its power consumption is moderate. Semi Dynamic flip-flops are a pulse triggered flip-flop which has two main blocks, level sensitive latch and pulse generator [4].

The conditional data mapping flip-flop (CDMFF) is one of the most efficient among them. It is one of the most efficient among the state-of-the-art designs. It uses an output feedback structure to conditionally feed the data to the flip-flop. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. But it has additional transistors added for the conditional circuitry which make the flip-flop bulky and cause an increase in power dissipation [9].

A flip-flop architecture which was introduced, named Cross Charge Control Flip-Flop (XCFF) has considerable advantages over SDFF and HLFF in both power and speed. Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load. A cross charge control flip flop (XCFF) has considerable advantages over SDFF and HLFF in both power and speed. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF. The effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design [8].

The Dual Dynamic node hybrid Flip-Flop (DDFF) eliminates the drawbacks of other designs and presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The Dual Dynamic node pulsed hybrid Flip- Flop (DDFF) is used to decrease circuit complexity, increasing operating speed and lower power dissipation. The glitch problems resulting from charge sharing could be reduced. An unconditional shutoff mechanism in DDFF overcomes the drawback of XCFF [1].The new dual dynamic flip-flop introduced in this paper has a clock gating technique which reduces further power. The existing design of counter includes static 2-input multiplexer where power consumption is of major concern. In order to magnify the performance improvement, we propose a 4-b Johnson up/down counter with dual mode logic. The normal multiplexer has been replaced by DML multiplexer where the counter could be operated both in static mode as well as dynamic mode.

The DDFF-ELM presents an area, power and speed efficient logic module. [1] .Note that in the revised model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed.

III. (a) PROPOSED ARCHITECTURE

The proposed hybrid Dual dynamic pulsed flip-flop (DDFF) architecture with clock gating technique acts both as static and dynamic circuits as in Fig.5. The operation of DDFF is based on the dynamic logic principles. This flip-flop requires two phases to operate based on the clock input to the circuit. The architecture and operation of the flip-flop is given in [1]. The architecture of DDFF with clock gating technique is shown in Fig. 1.

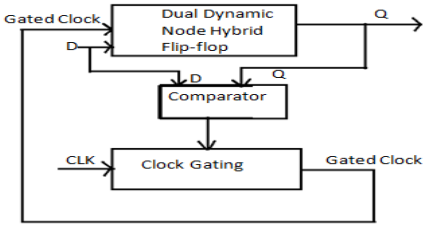


Fig. 1 DDFF with Clock Gating

To avoid unnecessary power consumptions like the power wasted by timing components during the time when the system is idle, the clock gating technique [12] has been developed. Clock gating means disabling the clock signal when the input data does not alter the stored data. The entire functional unit can be selectively set into sleep mode, or from the sequential/combinational circuit level where some parts of the circuit are in sleep mode while the rest of the block are operating.

The block contains two parts, the Dual dynamic flip-flop and the clock gating circuitry. The data signal arrives to the comparator and the DDFF flip-flop simultaneously. The comparator checks the output and the current data input from D.It checks if D and Q are equal, if it is not equal which means that the input has changed since the last comparison, then the clock gating circuitry will generate the active clock gating signal and the gated clock signal will be send to the DDFF flip-flop to trigger the storage. The input data will be passed through to the output. Otherwise, the entire system remains in the previous state.

(b) EMBEDDED LOGIC MODULE

SDFF has the capability to incorporate logic functions efficiently.The advantage of SDFF is fast and small implementation in terms of speed and area.The disadvantage is single node and more power dissipation[4]. But SDFF with embedded logic considered for comparative pulses.Double pulse set-conditional-reset flip-flop is capable of incorporating logic[7],but it has explicit pulse generator to generate two pulses from global clock.It also cause large power consumption even without any data transition.Stacked NMOS can be used in DDFF since no charge sharing.DDFF flipflop with embedded function(eg.OR) shown as in Fig.2.

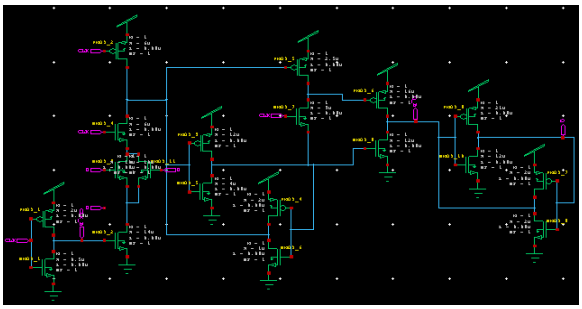


Fig.2 DDFF-ELM

IV. PROPOSED 4-B JOHNSON UP-DOWN COUNTER DML LOGIC

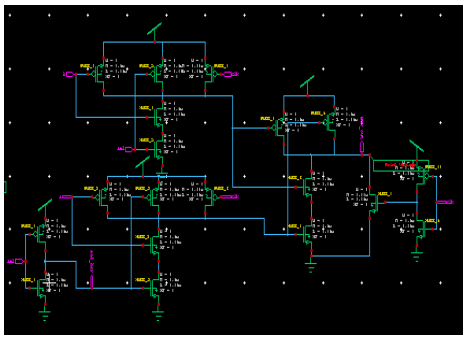


Fig.3 DML MUX

DML gates have a very robust operation in both static and dynamic at low supply voltages. It can be switched between static and dynamic modes of operation according requirements of the system. Thus support applications in which a flexible workload is required as shown in Fig. 10. In the static mode, DML gates consume very low energy with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation.

The basic concept behind the DML is to combine the traditional CMOS logic (or any other static logic) with a dynamic logic. Energy efficiency is achieved in the static DML mode at the expense of slower operation (Low Energy and Low Performance). However, the dynamic mode is characterized by high performance with increased energy consumption (High Energy and High performance).

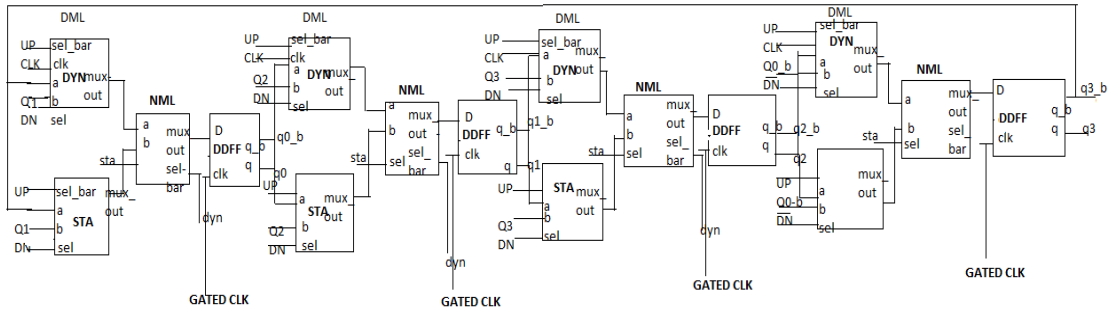


Figure 4: Up/down counter with Dual Mode Logic and Gated DDFF.

The 4-b Johnson up/down counter comprises of four dual dynamic node pulsed hybrid flip-flops (DDFF) and DML multiplexers as in Fig.4. The DDFF serves to be highly energy efficient with reduced delay. Initially all the flip-flops are in a reset condition. During up count, Q3-B is high (‘1’) on both the static and dynamic multiplexers of DML. Depending on the mode of operation been selected through the selection lines i.e, static or dynamic, inputs are given to the D-FF. Q0 is high (‘1’) and passes onto the next DML part of the counter. For each of the dual dynamic flip-flop, a clock gating technique is employed which will disable the clock when in sleep mode thereby reducing further power consumption.

Similarly the process continues depending on the counter operation (up/down).

V. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

Tanner EDA is a leading provider of easy-to-use, PC-based electronic based design automation (EDA) software solutions for the design, layout and verification of analog/mixed-signal integrated circuits, ASICs and MEMS. The result is simulated in TSPICE platform. Power consumption and the speed performances are discussed for HLFF, CDMFF, XCFF, SDFF and DDFF. The data driving power, clock driving power, D-Q delay are the major parameters considered as shown in Table 1. The comparison results show that DDFF serves to be an efficient flip-flop and it is well suited for modern high performance systems. The performance of 4-b Johnson up/down counter was analyzed by incorporating various design styles of flip-flops as shown in Table 2. The analysis reveals that the Dual Dynamic node pulsed hybrid Flip-Flop (DDFF) serves to be an efficient flip-flop structure by means of low power and high speed. DDFF with clock gating reduces further power. The simulation of 4-b Johnson up-down counter is been carried out using S-Edit of T-Spice. The counter with normal multiplexer consumes more power when compared to DML multiplexer. The speed of the counter is also been degraded. While operating the counter in DML (static) mode, it serves to be energy efficient whereas in DML (dynamic) mode, it serves to perform with high speed.The performance analysis of proposed design compared with different flip-flop styles and power consumption of flip-flop with ELM and power consumption of counter with DML logic and clock gating is provides in Table 1,2,3 respectively.

Table 1: Performance Analysis of Various Flip-Flop Structures

Flip-flop	Data driving power(µW)	Clock driving power(µW)	Latching power(µW)	Total power(µW)	D-Q delay(ps)
SDFF	124.5	22	252.18	398.68	295
HLFF	4.37	11.9	197.9	214.17	327.26
CDMFF	133.11	64.4	2.34	199.85	455
XCFF	10.6	7.06	177.01	194.67	351.06
DDFF	8.56	4.03	99.9	112.49	348.5
CG_DDFF (proposed)	0.45	1.1	13.8	15.38	1710

Table 2: Power Consumption of flip-flop with Embedded Logic

Embedded Flipflop	CLK power (µW)	Internal power (µW)	Total power (µW)
SDFF	**7.76**	**803.14**	**810.9**
DDFF-ELM	**3.46**	**642**	**645.46**

The performance of 4-b Johnson up/down counter was analyzed by incorporating various design styles of flip-flops as shown in Table 2.

The analysis reveals that the Dual Dynamic node pulsed hybrid Flip-Flop (DDFF) serves to be an efficient flip-flop structure by means of low power and high speed. The simulation of 4-b Johnson up-down counter is been carried out using S-Edit of T-Spice. The output waveforms generated were shown in fig 5,6.

Table 3: Performance Analysis of Counter with DML

COUNTER	NORMAL MUX	DML MUX(static)	DML MUX(dynamic)
Power(µW)	1022.47	664.73	670.17
Delay(ps)	507	490	486

Table 4: Power Consumption of counter with clock gating

DML	Power without Clock Gating(µW)	Power with Clock Gating(µW)
Static Mode	664.73	658
Dynamic Mode	670.17	664

Fig.4 Simulation waveform of counter with clock gating and DML MUX (dynamic)

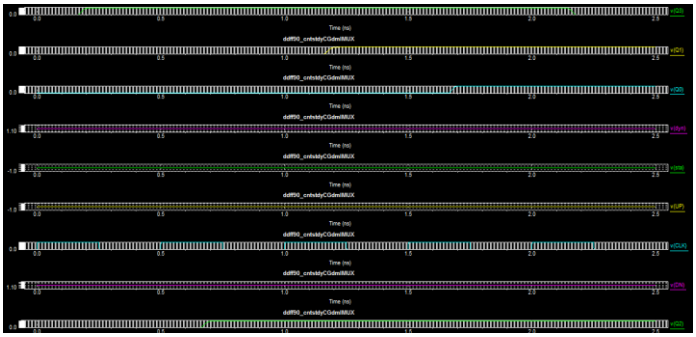
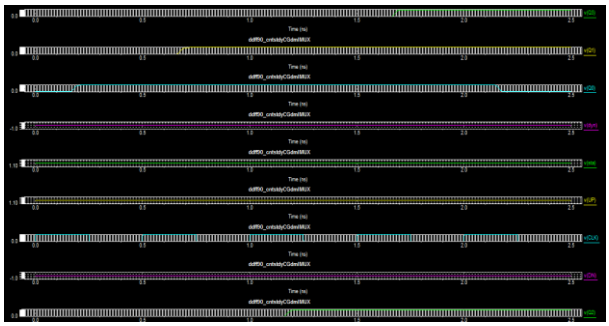


Fig.4 Simulation waveform of counter with clock gating and DML MUX (static)



VI. CONCLUSION

In this paper, a clock gating technique is applied to the dual dynamic flip-flop which reduce further power. To analyze the performance of flip-flop a 4-b Johnson up-down counter is used which uses normal MUX.But in this paper a 4-b Johnson up-down counter used with DML logic. DML logic can be switched between static and dynamic modes of operation according requirements of the system and to improve the speed performance. The power dissipation and speed performances of the flip-flop structures are considered. The DDFF and DDFF-ELM were analyzed. The DDFF eliminates the redundant power dissipation present in XCFF. The simulation result shows an improvement in power and delay parameters. 4-b Johnson up-down counter was used to highlight the performance parameters of the designs and to analyze the data activity at each bit position. Energy efficiency can be achieved by static DML mode and higher performance can be achieved by dynamic DML mode.

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