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Case study on the profit margin model of multi-site testing technology for semiconductors.

Voon C. Khoo IEng MIMechE [1]
[1](Asia e University, Malaysia)

Abstract: - Profit is the main goal of every business. Hence, investment on technology in a manufacturing firm ultimately aims at improving manufacturing efficiency to reduce manufacturing cost, thereby contributing to the profit of a firm. In this research, the author studied multi-site testing technology in the semiconductor testing industry to determine the contribution of technological advancements to profit. A profit model was developed based on economic theory with multi-site testing variables. The multi-site technology employed in this work was the pick and place handler, which is a popular technological approach. Five multi-site configurations were applied. These configurations were single-site, quad-sites, octal-sites, ×16-sites, and ×32-sites. A hypothesis was analyzed by using one-way ANOVA.

Keywords: *-profit margin, multi-sites testing, cost of test, testing technology, theory of the firm*

I. INTRODUCTION

The selling price of computers has decreased by 47% over the past 20 years. Profit margin during this period was maintained by reducing fabrication cost. However, from early 2012 onwards (Bao, 2003), fabrication cost has ceased to be the deciding factor for profit margin in semiconductor manufacturing. Fabrication cost has been replaced by testing cost, as shown in Figure 1. The cost of testing increases with the number of transistors in each chip. Thus, testing cost should be reduced in the future. The selling price of electronic devices continues to decline, thereby hindering manufacturers from maintaining profit margins and remaining competitive in the market. Thus, testing cost has become a major concern requiring urgent attention.

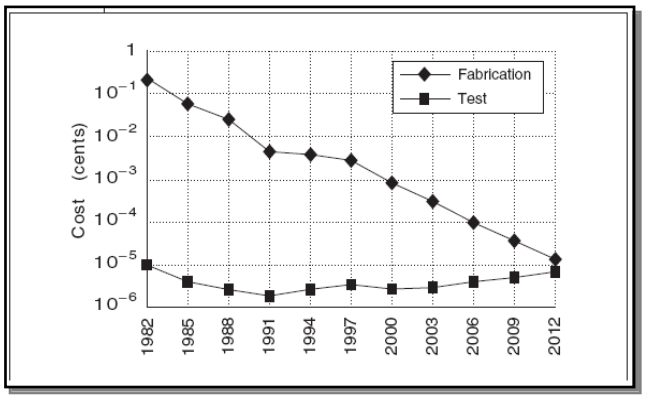

Figure 1 Cost of Testing a Transistor Approximates the Cost of Fabricating It (Bao G., 2003)

Consequently, a reduction in testing cost has become the common goal of semiconductor manufacturers worldwide. Failure to reduce testing cost can cause a semiconductor chip manufacturing company to lose its competitiveness in the market. An effective method by which to reduce testing cost is to decrease testing time. Decreasing testing time also increases testing throughput. To achieve this objective, the performance and speed of the test equipment have to be improved. Therefore, the chip-transfer time and chip-testing sequence should be developed to test semiconductor chips rapidly.

To improve the testing process, numerous new technologies have been developed. However, the advancement of technology increases capital investment in equipment. The failure of a new technology to provide the expected throughput outcome increases testing costs. Therefore, studying the efficiency of equipment in relation to capital investment is vital in ensuring that the semiconductor industry is geared toward the right direction and incurs lower costs in testing while maintaining adequate profit margins.

Numerous models for testing cost have been previously developed to calculate the capability of technology to increase testing throughput as well as to determine the actual cost involved in testing a semiconductor chip. However, these models do not consider profit margin in the calculation. Profit margin is crucial in determining the amount to spend on testing. Thus, this factor should be included in the calculation. The inclusion of profit margin in the calculation of testing cost determines the capability of the test equipment to achieve the expected testing cost. Therefore, as an initial effort to address the aforementioned research gap, this study presents a testing cost model that considers profit margin in the calculation.

II. DEVELOPMENT OF PROFIT MARGIN MODEL

Cost of Test Model

The cost-of-test model in this research was developed based on average cost theory, as shown in Equation 1. Average cost theory involves two elements: total cost and production output.

$$\text{Average Total Cost (ATC)} = \frac{\text{Total Cost (TC)}}{\text{Output (Q)}} \quad (1)$$

A. Total Cost

According to the average total cost theory, the total cost included of fixed cost and the variable cost. For the multi-sites testing aspect, the variables which affected the total cost are shown in table 1 as below.

i. Fixed Cost

Whereby the fixed cost included of equipment depreciation cost (Dep) which contain of the tester cost and the test handler cost. Equation 2 was developed to calculate the equipment depreciation cost which span over five years from it purchase value to zero-cost.

$$\text{Dep} = \left(\frac{\text{Tester Cost} + \text{Handler Cost}}{5} \right) \div 12. \quad (2)$$

Table 1: MULTI-SITES TESTING VARIABLE FOR TOTAL COST.

Total Cost	
Fixed Cost	**Variable Cost**
Depreciation Cost i. Tester Cost ii. Test Handler Cost	**Bad Parts Cost**
Direct Labor Cost i. Operator Salary ii. Technician Salary	
Overhead Cost i. Management Cost - Manager's salary - Supervisor's salary - Engineer's salary ii. Facility cost - Electricity cost, - compress air cost etc iii. Floor space cost iv. Maintenance cost - Wear and tear parts - Consumable parts etc v. Test accessories cost - Test socket/contactor - Test Load board	

The second variable which affecclted the fixed cost is the direct labor cost (DL). The direct labor (DL) cost is the monthly salary of employees who directly contributes to the production output, such as operators and technicians. Direct labor cost is expressed in Equation 3:

$$\text{Direct Labor Cost per month} = \left(\text{Operator salary per month} \times 3\right) + \left(\text{Technician salary per month} \times 1.5\right) \quad (3)$$

For the operator variable, each test-equipment setup requires one operator, and thus, three operators are needed each day to cover three production shifts. For one shift, only one operator is required. To standardize the equation for ease of understanding, three shifts are used in this study.

For the technician variable, one technician can support two test-equipment setups. Therefore, only a half the cost is needed per test-equipment setup. To cover three production shifts, only 1.5 technicians are needed.

Operator and technician wages are based on a report published by JobStreet.com. (Cited: 11 April 2012). In this study, the average wage is used as a reference for the aforementioned positions.

In addition, the Overhead (OH) cost is the cost incurred during production aside from equipment depreciation and direct labor costs. Overhead cost includes the following.

- Management Cost includes the monthly wages of the manager, supervisor, and engineer, which are considered as indirect labor costs. Wages data are based on a JobStreet.com report (cited: 11 April 2012). Equation 4 shows management cost calculation:

$$\text{Management cost} = \text{Manager's Salary} + \text{Supervisor's Salary} + \text{Engineer's Salary} \quad (4)$$

- Facility Cost is the monthly utility cost of electricity, compressed air, and so on.
- Floor-Space Cost (FPS) is the cost of the area occupied by the test-equipment setup. Equation 5 shows the calculation of floor space cost:

$$\text{FPS} = \left(\frac{\text{(Selling Price)}}{3000}\right) \text{X} \begin{array}{c}\text{Test Equipment}\\ \text{floor space area}\\ \text{(Sq-Ft)}\end{array} \quad (5)$$

In this study, the calculation of floor-space cost is based on the Malaysian Government Valuation and Property Service Department Report 2011. The 2011 "Detached House Pricing" is adopted as a reference for calculating price per sq. ft. Test equipment setup floor space costs are then calculated as the X number of area sq. ft. needed multiplied by the per sq. ft. pricing, as shown in Equation 5.

- Maintenance Cost is the cost spent in one month to maintain the test equipment, such as wear-and-tear part cost, consumable part cost, and so on. The study estimates maintenance cost at 5% per year of the test equipment cost.
- Cost-of-Test Accessories includes the test contactor and load board, which are described as follows:
- Load Board/Probe Card is the electronic printed circuit board used for interfacing between the tester and the test handler.
- Test Contact Socket is the mechanism used to connect the semiconductor device to the load board.

ii. Variables Cost

Another factor identified as part of the total cost calculation that has an effect on the test yield is the variable cost. From the research point of view, the variable cost is categorized as a changeable cost because it is not fixed, and it will change when the testing yield is modified.

The variable cost that needs to be included is the bad-part cost based on the test cost model developed by Rivoire (2003). The bad-part cost is imperative in this research, particularly when dealing with multi-site configurations, because the developed model will be validated using this configuration. When changes are implemented during testing, they may affect the consistency of the testing yield, which depends on multi-site repeatability efficiency.

To include the bad-part cost into the total cost equation, an equation has to be derived to calculate the cost of bad parts. The first step in deriving the bad-part cost equation is to imply the appropriate equation that can calculate the quantity of bad parts. Equation 6 is derived for this purpose.

$$\text{Number of bad part} = \text{Total Input X } \left[100\% - (\text{Testing Yield})\right] \quad (6)$$

Based on Equation 6, total incoming chip quantity is multiplied by the bad part yield, which can be obtained by deducting the testing yield from 100%. The testing yield is the tested good part percentage that can be obtained from Equation 7:

$$\text{Testing yield \%} = \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (7)$$

Finally, to calculate the cost of the tested bad parts, the ASP of a particular type of semiconductor chip is multiplied with the number of bad parts obtained from Equation 6. Therefore, Equation 8 is derived to determine the total cost of tested parts.

$$C_{Pkg} = \text{ASP} \left[\text{Total Input X} \left(\text{ Bad part \% } \right) \right] \quad (8)$$

where:
- CPKg is the cost of bad parts;
- ASP is the average selling price;
- Total Input is the total input of semiconductor chips; and
- Bad Part % is the tested bad chips obtained by deducting the testing yield from 100%.

All costs have been discussed thoroughly to facilitate total cost calculation. Therefore, by putting together all the equations, Equation 9 is derived to demonstrate how the total cost has been integrated:

$$\text{Total Cost} = \text{Dep} + \text{DL} + \text{OH} + C_{Pkg.} \quad (9)$$

Another element incorporated in average cost theory for the developed model is production output. A detailed discussion of this element is provided in the following subsection:-

B. Production Output

Production output consists of three fundamentals: testing output (throughput), testing yield, and the equipment utilization percentage. Detailed explanations for these fundamentals are as follows.

$$UPH_{good} = \frac{3600 \text{ X N}}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1))} \text{ X } \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (10)$$

Equation 10 was developed to calculate the production throughput whereby the throughput obtained is the tested good product by take into account the testing yield whereby the testing yield mean that the percentage of tested good. The equation of testing yield % is shown in equation 7 in this paper.

The equation 10 was integrated with the Multi-sites efficiency (MSE) as well so that the comparison between the multi-sites versus the multi-sites efficiency (MSE) can be obtained, but in this paper will not analyze of this hypothesis and will reserve for next paper publication.

To integrate the MSE into the equation, the throughput equation from Evans (1999) as shown in equation 11 need to further enhance. Following discuss step by step on how the MSE was integrated into the throughput equation.

$$UPH_{insertions} = \frac{3600 \text{ x n}}{t_{ms} + i_{ms}} \quad (11)$$

where:
- tms is the multi-site test time, that is, the time spent to complete the testing of a semiconductor chip.
- ims is the multi-site indexing time, that is, the semiconductor chip exchange time within the tested chip replaced with a new untested chip.
- n is the number of test sites, that is, the number of semiconductor chips tested in a single contact.

To achieve the integration with the MSE, the throughput equation developed by Evans (1999), shown as Equation 11, is enhanced by integrating the MSE model developed by Kelly (2008). The MSE proposed by Kelly is presented as Equation 12:

$$MSE = \left(1 - \frac{\Delta t}{\Delta N(t_1)}\right).100\% \qquad (12)$$

where:
- Δt is the change in testing time between single-site and multi-site testing; and
- ΔN is the number of different test sites between single-site and multi-site testing.

Equation 12 is further derived, as shown in Equation 13.

$$MSE = \left(1 - \frac{(t_{MS} - t_1)}{(N-1)(t_1)}\right).100\% \qquad (13)$$

where:
- t_{MS} is the multi-site test time, and t1 is the single-site test time; and
- N is the number of test sites for multi-site testing.

The test handler affects testing throughput. Therefore, the test handler indexing time has to be included as part of the MSE equation. In doing so, Equation 14 is derived by including the indexing time (i), as follows:

$$MSE = 1 - \left(\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N-1)(t_1+i_1)}\right).100\% \qquad (14)$$

For the integration of the equations to work, one must have prior understanding of the relationship between the throughputs and MSE. To determine the relationship between MSE and multi-site, the variables of MSE, which is related to the throughput, need to be understood. Equation 11 and Equation 14 show that the multi-site test time (t_{ms}) and multi-site indexing time (i_{ms}) are common variables in both equations.

In Equation 14, t_{MS} and i_{MS} represent multi-site test time and indexing time. Therefore, to clearly derive the relationship between t_{ms} and i_{ms} in relation to MSE, the integration process shown in Figure 2 is carried out.

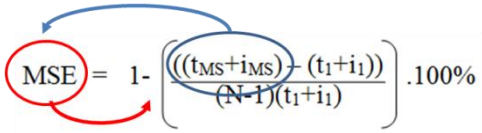

Figure 2 Deriving the Relationship between t_{ms} and i_{ms} with MSE

As Figure 2 illustrates, t_{ms} and i_{ms} move to the left side of the equation, whereas MSE moves to the right side. The final computation for the equation of t_{ms} and i_{ms} in relation to MSE is derived and shown in Equation 15.

$$(t_{MS} + i_{MS}) = (1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1). \qquad (15)$$

Finally, Equation 15 is integrated into Equation 11 to obtain the computation for testing throughput, which includes MSE as part of the calculation. Figure 3 below shows the computation of the integration, and the

complete integration is illustrated in Equation 16:

$$UPH_{insertions} = \frac{3600 \times n}{t_{ms} + i_{ms}}$$

$$(1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1)$$

Figure 3 The Computation of the Integration of Equation 15 into Equation 11

$$\mathbf{UPH_{insertions}} = \frac{\mathbf{3600\ X\ N}}{\mathbf{((1\text{-}MSE)(N\text{-}1)(t_1+i_1)\ +\ (t_1+i_1)),}} \qquad (16)$$

where:
$UPH_{insertions}$ are represented by the testing output in one hour.

C. Equipment Utilization (U)

Equipment utilization percentage refers to the percentage by which the test equipment is used in producing output. When the test equipment is 100% utilized, then no cost is lost. The aforementioned cost refers to the total cost, as indicated in Equation 9. When equipment utilization achieves a higher percentage, the cost becomes cheaper. By contrast, when utilization percentage begins to decrease, then the cost increases (Horgan, 2004).

Given that equipment utilization percentage affects the total cost, then the former must be included in Equation 9. Therefore, the total cost equation, which involves equipment utilization percentage, is depicted in Equation 17.

$$\text{Total Cost per month} = \frac{(Dep + DL + OH + C_{Pkg})}{U} \qquad (17)$$

The total cost obtained from Equation 17 is the monthly testing expenditure. However, the testing throughput is calculated based on the hourly production output. Therefore, to obtain the total cost per hour, Equation 17 has to be further derived, as shown in Equation 18.

$$\text{Total Cost per hour} = \frac{\left(\frac{Dep + DL + OH + C_{Pkg}}{729.6}\right)}{U} \qquad (18)$$

Where the total cost is divided by 729.6 to obtain the hourly cost; and 729.6 is the total number of production hours in one month.

After all the equations and variables for average cost theory are defined, the next step is to integrate all the equations into average cost theory to derive the cost of the model. The integration is illustrated in Figure 4:

$$\frac{\left(\frac{Dep + DL + OH + C_{Pkg}}{729.6}\right)}{U}$$

Equation 18

$$\text{Average Total Cost (ATC)} = \frac{\text{Total Cost (TC)}}{\text{Output (Q)}}$$

Equation 2.1

$$\frac{3600\ X\ N}{((1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1))}\ X \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}}\ X\ 100\right)$$

Equation 10

Figure 4 The Integration of Equations 18 and 10 into Equation 1.

As shown in Figure 4, the average cost in Equation 1 is integrated with Equation 18, which is the total cost in one hour, and Equation 10, which is the total number of good chips tested in one hour.

The final cost of test model is then integrated, as shown in Equation 19:

$$CPU_{GOOD} = \frac{\left(\frac{\left(\frac{Dep + DL + OH + CPkg}{729.6}\right)}{U}\right)}{\left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1) + (t_1+i_1))}\right) \times \left(\frac{Total\ Good\ Device}{Total\ Incoming\ Device} \times 100\right)} \quad (19)$$

Cost of Test Profit Model

Following further discuss of the cost of test into the Profit Theory whereby the Economic Profit Theory is shown in equation 20:

$$Profit = Total\ Revenue\ (TR) - Total\ Cost(TC) \quad (20)$$

As shown in Equation 20, two elements are incorporated in profit calculation, namely, total cost and total revenue. Total cost can be derived from the cost of test model (Equation 19). Total revenue is discussed in this section. To clearly explain the profit margin model, the discussion is divided into three subsections. The first subsection explains how total cost is derived from Equation 19. A discussion of the total revenue follows in the second subsection. The final section discusses the development process of the cost-of -test profit margin model.

i. Total cost from Equation 19

As indicated in ***Equation 1***, the total cost is one of the elements of the average cost. The average cost equation is used to derive the relationship of the total cost with the cost of test because the cost of test equation is based on average cost theory. The derivation process is shown in Figure 5.

$$Average\ Total\ Cost\ (ATC) = \frac{Total\ Cost\ (TC)}{Output\ (Q)}$$

Figure 5 Derivingthe Total Cost through Equation of Average Cost.

As shown in Figure 5, to derive the total cost equation through average cost theory, the output has to move from the left side of the equation to its right side, and the dividend becomes the multiplier. The total cost formula in the relation to the average is derived and shown in ***Equation 21***.

$$Total\ Cost = Average\ Total\ Cost \times Output. \quad (21)$$

As discussed earlier, the cost of test is equal to the average cost; therefore, Equation 21 is further derived and expressed as Equation 22.

$$Total\ Cost = Cost\ of\ Test \times Output. \quad (22)$$

The total cost is equal to the cost of test multiplied by the production output, which, in this case, is the testing throughput. The variables in Equation 19 and Equation 10 are integrated with Equation 22, as illustrated in Figure 6, and further derived as shown in Equation 23.

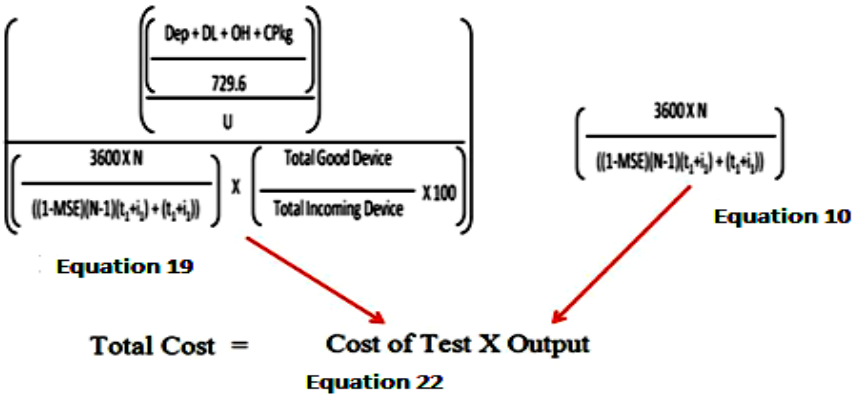

Figure 6 The Integration of Equation 19 and Equation 10 into Equation 22

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6} \right)}{U} \Big/ \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1) + (t_1+i_1))} \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100 \right) \right) \right) \times \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1) + (t_1+i_1))} \right) \quad (23)$$

Equation 23 is further simplified by canceling the unit per hour (UPHinsertion) equation, as shown in Equation 24.

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6} \right)}{U} \Big/ \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1) + (t_1+i_1))} \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100 \right) \right) \right) \times \left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1) + (t_1+i_1))} \right) \quad (24)$$

The final equation for the total cost calculation is shown as Equation 25.

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6} \right)}{U} \Big/ \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100 \right) \right) \quad (25)$$

Equation 25 indicates that the equipment utilization percentage and the good unit yield influence the total cost. After deriving the total cost equation, the discussion of total revenue theory in the following section:-

ii. Total Revenue

Base on theory of the firm, total revenue is derived from market demand quantity multiplied by product selling price (McKenzie, 2006). This relationship is expressed in Equation 26.

$$\text{Total Revenue} = \text{Demand} \times \text{Selling Price}. \quad (26)$$

Demand refers to the quantity of semiconductor chips needed by the market, and the selling price is the ASP for a particular semiconductor chip. For this study, demand is determined as the same value of the testing throughput for easy calculation.
Both elements that influence profit have been discussed, and the following section describes in detail the development process of the cost of test profit margin model.

iii. Development Process of the Cost-of-Test Profit Margin Model

Profit is the difference between the total cost and the total revenue (Kling, 2005). The profit equation can be expressed as Equation 20 where the profit is equal to the total revenue minus the total cost.
Based on Equation 20, Equation 25 and Equation 26 are integrated, as shown in Figure 10; and the final test profit margin model is developed, as shown in Equation 27.

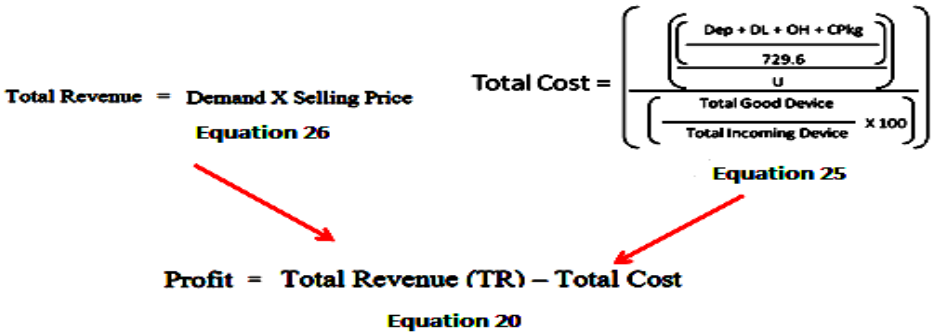

Figure 10 The Integration of Equation 26 and Equation 25 into Equation 20.

$$\text{Profit} = \left[\text{Demand X Selling Price}\right] - \left[\frac{\left[\frac{\left[\frac{\text{Dep + DL + OH + CPkg}}{729.6}\right]}{U}\right]}{\left[\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100\right]}\right] \quad (27)$$

The integration is successfully shown in Equation 427, thus enabling calculation of the profit margin of the cost of testing for research hypothesis.
Changing the demand and testing throughput to produce the required demand affects the test equipment utilization percentage and the required test equipment to produce that demand, therefore Equation 27 needs to be further improved to solve this problem. The following discussion of the equations considers the utilization percentage and the change in the number of test equipment when the required demand is modified.

To simulate different production outputs or required demands, calculating the equipment utilization percentage based on testing output increment across different test-site setups is necessary.
The total cost is affected by the equipment utilization percentage and good unit yield. Therefore, the equipment utilization percentage for the different testing throughputs can be calculated using Equation 28.

$$\text{U\% for Production Output (U\%O)} = \frac{\text{Production Output}}{\text{UPH}_{\text{insertion}}\text{ (Perfect Condition)}} \times 100, \quad (28)$$

where:
The production output (required market demand) is divided by $UPH_{insetion}$ in perfect condition. $UPH_{insertion}$ in perfect condition indicates that the maximum testing throughput that the test equipment can produce in one hour can be obtained with Equation 16 via 100% MSE.
However, Equation 16 cannot provide an accurate calculation because when the test equipment is 100% utilized, it requires an additional setup to produce the additional testing throughput. To solve this problem, the utilization percentage equation in Equation 28 should be further enhanced, as shown in Equation 29.

$$\text{Actual U\% for Production Output (AU\%O)} = \frac{\text{U\%O}}{\text{Number of Test Equipment}} \quad (29)$$

where the actual utilization percentage (AU%O) can be calculated by dividing the utilization percentage per output (U%O) with the number of test-equipment setups needed to produce the required testing output so that the actual utilization percentage per test-equipment setup can be obtained.
When the first test equipment reaches 100% utilization, additional test equipment is needed to produce the additional testing output, and the increment of the number of test equipment depends on the required output.
To obtain the cost of good unit based on the increment of testing output demand, the actual utilization percentage (AU%O) and the required number of test equipment (NOTE) have to be integrated into the total cost in Equation 25. The integration shown in Figure 7 and the new total cost equation, which considers the AU%O and NOTE, are derived in Equation 30.

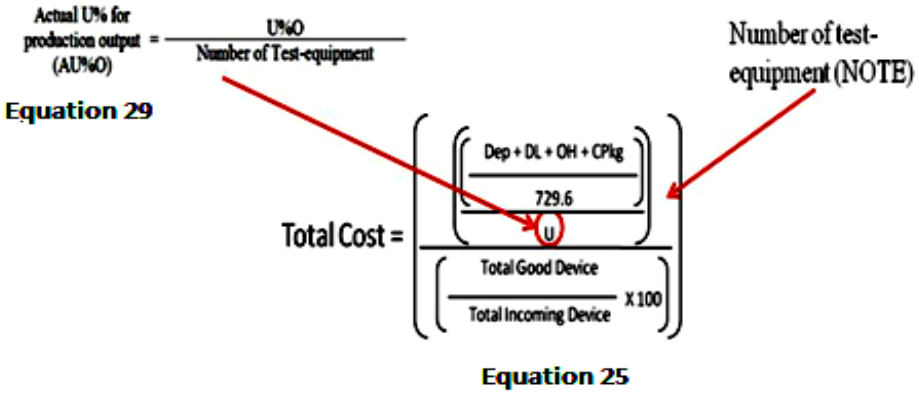

Figure 7 The Integration of Actual Utilization Percentage and NOTE into Equation 25.

$$\text{Total Cost} = \left(\frac{\left(\frac{\text{Dep + DL + OH + CPkg}}{729.6} \right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100} \right)} \right), \quad (30)$$

where NOTE is the number of test-equipment setups needed for a particular production output, and the utilization percentage (U) is replaced with the actual utilization percentage based on the required output (AU%O).
Finally, the profit margin equation, which includes AU%O and NOTE, is derived, as shown in Equation 31:

$$\text{Profit} = \left[\text{Demand X Selling Price} \right] - \left(\frac{\left(\frac{\text{Dep + DL + OH + CPkg}}{729.6} \right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100} \right)} \right) \quad (31)$$

III. PICK AND PLACE TEST HANDLER

Pick-and-place testing handling is one of the widely used methods of testing multi-sites. In this process, the semiconductor chip is already singulated from the lead frame to become an individual chip. The chip is placed on a Jedec tray to be carried from the assembly equipment to the test equipment. Figure 8 shows a photograph of Jedec trays.

Figure 8 Sample Jedec trays.

The Jedec tray is loaded with semiconductor chips and then placed into the pick-and-place handler in Area 1, as shown in Figure 9.

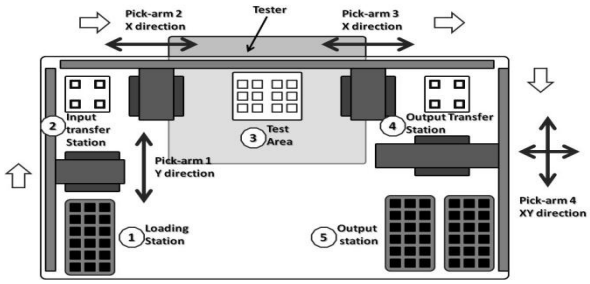

Figure 9 Process flow of pick-and-place testing handling.

Pick-arm 1 transfers the chips from the tray to the input transfer station. From the input transfer station, pick-arm 2 moves the chips to the test area for testing. The pick-and-place testing handling method is different from the two previous methods, in which the tester is at the bottom and the test socket/contactor is facing up. Moreover, pick-arm 2 punches the device down instead of up to connect it with the test socket/contactor. The tested chips are then placed on the output transfer station by pick-arm 3. Finally, pick-arm 4 removes the tested chips from the output transfer station and sends them to the output station. The good and bad chips are sorted according to the test results. Figure 10 displays the test area for pick-and-place testing handling.

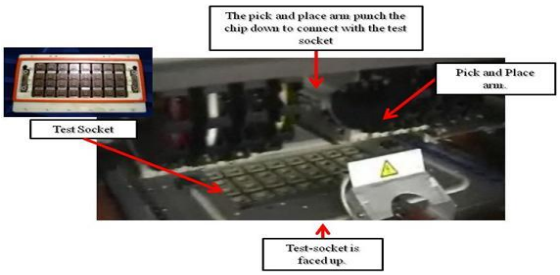

Figure 10 Test area for pick-and-place testing handling.

The test site configuration setup for the case study is explained in the subsequent section.
The pick-and-place test equipment can be configured from single-site to X32-sites. The test sites are configured to obtain data for the case study from single-site to X32-sites. Figure 11 displays a photograph of the pick-and-place test equipment test sites that can support X32-sites.

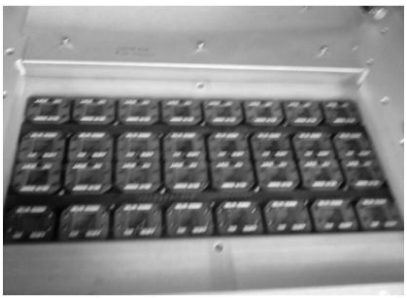

Figure 11 Pick-and-place test sites.

The standard layout of the test site for the pick-and-place test equipment is configured in four columns and eight rows to obtain X32-sites. With such flexibility, the test site can be configured to single-site, quad-sites, octal-sites, X16-sites, and X32-sites. The details of the configurations are described below. From the standard test site configuration (Figure 12), the experiment first configures the test handler to pick up only one chip and to perform single-site testing to simulate the indexing and test times of the conventional testing method. Figure 13 depicts the single-site configuration (gray color indicates the test site used for testing).

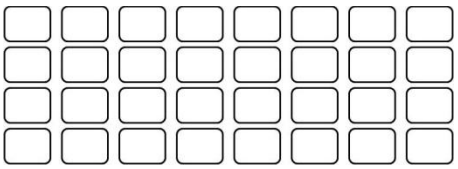

Figure 12 Standard layout of X32-sites.

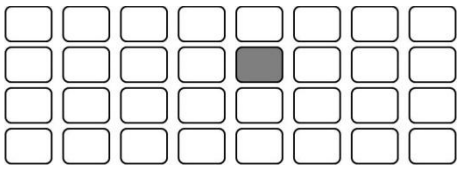

Figure 13 Layout of single-site.

Figures 14 and 15 show the configuration of quad-sites and octal-sites, respectively.

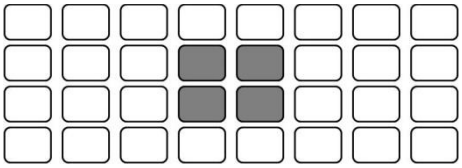

Figure 14 Layout of quad-sites.

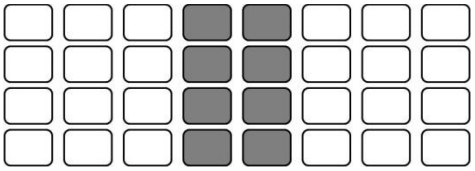

Figure 15 Layout of octal-sites.

The test handler is configured to X16-sites (Figure 16) and X32-sites (Figure 17) when the quad-site and octal-site tests are completed.

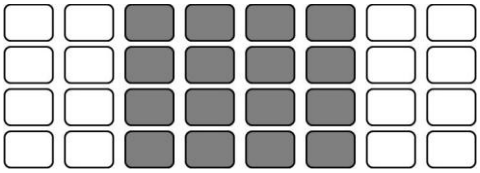

Figure 16 Layout of X16-sites.

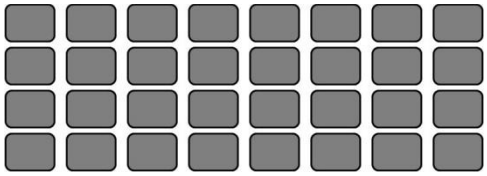

Figure 17 Layout of X32-sites

The configurations of test sites are defined. The results of the analysis are discussed in the section that follows.

IV. ANALYSIS RESULT

Cost of Good Unit

This study considers pure indexing time only and rejects any indexing time slowed down by external factors, including the carrier transfer process, loading and unloading process, equipment jamming, and delay caused by slowing of pick-arm 1. Production data are only accepted if no external factor, including handler and tester downtimes, is identified.

This study focuses on only the area shown within the circle in Figure 18.

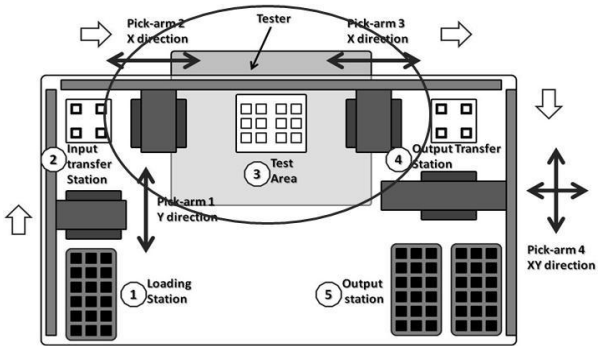

Figure 18 Focus area of this research.

The indexing time is considered valid if no waiting time exists between the exchange times for the device being tested as it is replaced with a new device before testing. However, the indexing time is considered invalid given external factors that cause immediate replacement of a new chip after the device is completely tested.
The test time is considered valid if no external factors, including tester downtime and chip contacting problems, cause a high rejection rate of the tested chip.
The data size of the 30 sets of production lots for each test site configuration (single-site, quad-sites, octal-sites, X16-sites, and X32-sites) must be collected to gather sufficient data for the cost-of-test study. Each data set contains 100 trial runs of the test equipment setup. Thus, the 30 data sets contain 3,000 test equipment trial runs. Five test site configurations are employed in both case studies. Therefore, 30 sets are used for each test site setup. The five test site configurations contain 150 data sets, including 15,000 trial runs on test equipment.

The fixed costs for this case study are tabulated in Table 2.

Table 2: FIXED COSTS

Variables	Cost (RM)
Depreciation cost/month	49500
Direct labor cost/month	7843
Overhead cost/month	181999

The cost of bad parts is calculated by using Equation 8, which involves an ASP of RM4.95 for the logic device. The cost of bad parts is affected by the testing yield. Table 3 depicts the summary of the cost of bad parts.

Table 3: COST OF BAD PARTS

Test site configurations	Cost of bad parts (RM)
Single-site	63.61
Quad-sites	110.29
Octal-sites	141.61
X16-sites	192.55
X32-sites	163.45

The results of testing throughput for pick-and-place test equipment are summarized in Table 4.

Table 4: TESTING THROUGHPUT FOR PICK-AND-PLACE TEST EQUIPMENT

Test site configurations	Throughput
Single-site	2659
Quad-sites	4126
Octal-sites	4447
X16-sites	4576
X32-sites	3825

Testing yield is one of the factors that affect testing cost. Table 5 shows the testing yield percentage data collected from the pick-and-place test equipment setup.

Table 5: AVERAGE TESTING YIELD PERCENTAGES

Test site configurations	Average Testing Yield (%)
Single-site	99.52
Quad-sites	99.46
Octal-sites	99.36
X16-sites	99.15
X32-sites	99.14

After all the required variables are obtained, the cost of good units is calculated by using Equation 19. The summary is tabulated in Table 6.

Table 6: COST OF GOOD UNIT.

Test site configurations	Cost of Good Unit (RM)
Single-site	0.0670
Quad-sites	0.0436
Octal-sites	0.0410
X16-sites	0.0409
X32-sites	0.0488

Cost of Test Profit

After obtaining the cost of testing for the entire test-site setup, the next step is to calculate the profit margin for the pick-and-place test equipment.

The main elements involved in the profit-margin calculation are total revenue and total cost, as shown in Equation 20. Total revenue is calculated by the selling price multiplied by the selling output. In this study, the ASP list published by the World Semiconductor Trade Statistics and identified by Turley (2009) is used in the total-revenue calculation. The device-type used in this Case Study is the logic semiconductor, and the selling price is USD 1.50, which is equivalent to RM4.95 per chip.

As stated in the previous chapter, the study needs to simulate mass production cost to obtain the profit margin for the test-equipment setup. To achieve this, the total cost of the production output from 1,000 to 23,000 chips per hour is calculated based on Equation 31.

In the first step in simulating the mass production cost of test, this study determines the number of test equipment needed to test the required production output across all test-site configurations. The number of test equipment is determined by referring to the utilization percentage of the test equipment. Once the utilization percentage reaches more than 100%, then additional test equipment is needed. The utilization percentage based on the production output is calculated using Equation 28. An example of the calculation for single-site testing is shown as follows:-

$$\text{U\% for production output (U\%O)} = \frac{1{,}000}{2{,}659} \text{ X } 100$$

$$= 38\%.$$

From the aforementioned example, the utilization percentage is 38%. Thus, only one test equipment setup is needed.

To obtain the actual utilization percentage for the test equipment, Equation 29 is developed. An example of the calculation is shown using single-site testing with 6,000 production output units, as follows:-

$$\text{Actual U\% for production output (AU\%O)} = \frac{226\%}{3}$$

$$= 75\%.$$

From the given example, the utilization percentage for a single-site pick-and- place equipment is 226% to produce 6,000 units. Three test equipment units are required to produce 6,000 units of output given that the utilization percentage is over 200%. Only one test-equipment is required when the utilization percentage is below 100%. Two tests equipment are required when the utilization percentage is below 200%.Three tests equipment are required when the utilization percentage is below 300%.

Table 7 shows the utilization percentage and the number of test equipment units needed for a production output of 1,000 to 23,000 units across all test site configurations.

After obtaining the number of handlers and actual utilization percentages, this study calculates the total cost for the entire production output across all test-site configurations.

Equation 30 issued to calculate the total cost. An example of the calculation for a single-site testing with 9,000 unit production outputs is shown as follows:-

$$\text{Total Cost} = \left(\frac{\left(\frac{129372.43}{729.6} \right) \text{X } 4}{85\%} \right) \Bigg/ 100\%$$

$$= \text{RM838}.$$

Table 7 shows that four test-equipment units are required to produce an output of 9,000 units per hour, and that the utilization percentage per test equipment is 85%. For a fair comparison, good-unit yield percentage is fixed at 100%.

The given example shows a cost of RM838 per hour to produce 9,000 chips.Table 8 shows the total cost of the entire production output across all test-site configurations for the pick-and-place test equipment.

To determine the cost of good units using simulation from 1,000 to 23,000 chips per hour, this study divides the total output of 27,600 by the grand total cost to obtain the average cost per unit. An example of the calculation for single-site testing is shown as follows:-

$$\text{Cost of Good Units} = \frac{23,\ 353.11}{27,600}$$

$$= \quad 0.0846.$$

As shown in Table 8, the single-site setup requires RM0.0846 to test a semiconductor chip, and quad-site setup requires RM0.0612. Octal-site expense per chip is RM0.0606. The cost is RM0.0607 for the X16-site testing, and RM0.679 for the X32-site testing.

After obtaining the total cost of the simulation of production output shown in Table 8, this study calculates the profit margin of the simulation using Equation 31. The calculation of the profit is summarized in Table 9:-

Hypothesis: Multi-site versus Profit Margin Improvement

Refer to Table 9 for the pick-and-place test-equipment profit summary for the production output simulation from 1,000 to 23,000. Analysis for the hypothesis is provided in the following sections:-

The hypothesis for the profit-margin analysis is as follows.

H0: Improvement of the test site has no effect on the improvement of the profit margin.

H1: Improvement of the test site has an effect on the improvement of the profit margin.

Table 10: ANOVA Results for Profit Margin

ANOVA Table

	SS	df	MS	F
Between	0.40	4.00	0.10	0.04
Within	287.57	110.00	2.61	
Total	287.97	114.00	2.53	

For the profit margin ANOVA, the degree of freedom between is 4 and 110, with an alpha level of 0.05. The critical value obtained is 2.4542 (www.danielsoper.com/statcalc3/calc.asp.cited: 8 September 2012).The F-value obtained from the analysis is 0.04, which is lower than the critical value. In this case, the null hypothesis is accepted; and the study concludes that improvements on test sites for pick-and-place test-equipment setups have no significant effect on the profit-margin improvement.

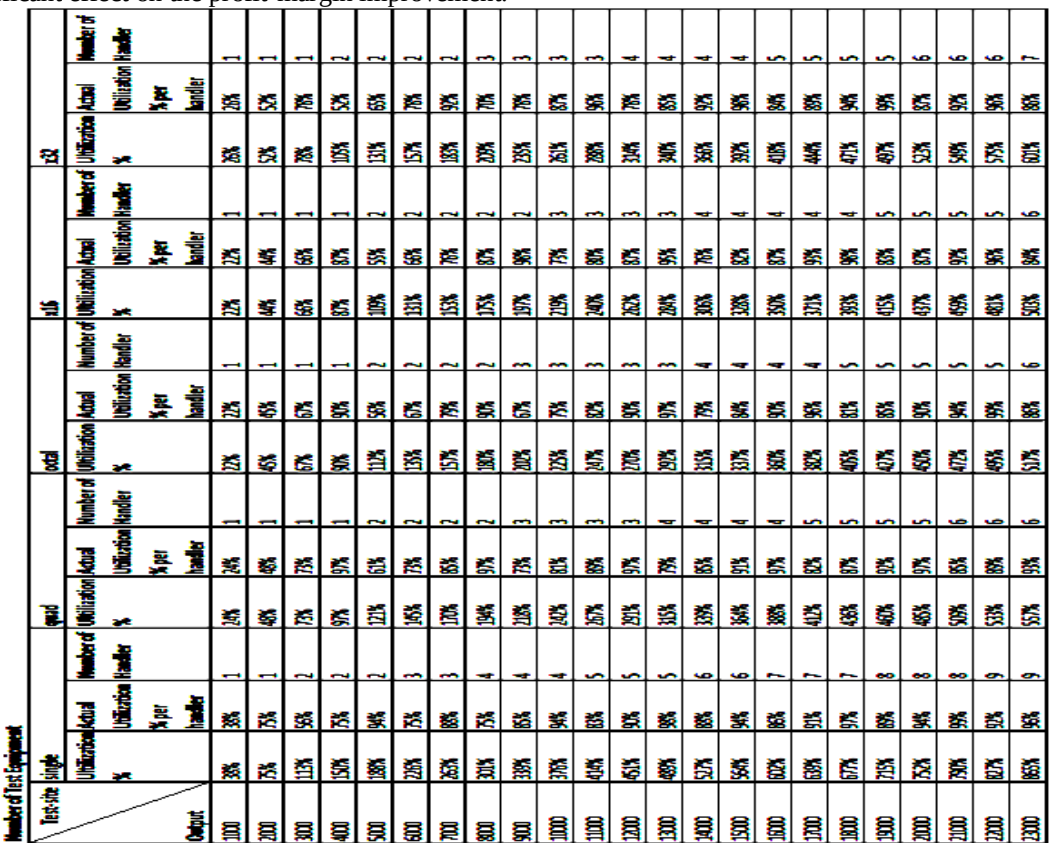

Table 7: Increment of Test Equipment Units Based on

Total Cost

Output	single-site	Average Cost	quad-sites	Average Cost	octal-sites	Average Cost	x16-sites	Average Cost	x32-sites	Average Cost
1000	MYR 471.46	MYR 0.47	MYR 738.42	MYR 0.74	MYR 805.56	MYR 0.81	MYR 849.12	MYR 0.85	MYR 707.18	MYR 0.71
2000	MYR 235.73	MYR 0.12	MYR 369.21	MYR 0.18	MYR 402.78	MYR 0.20	MYR 424.56	MYR 0.21	MYR 353.59	MYR 0.18
3000	MYR 628.61	MYR 0.21	MYR 246.14	MYR 0.08	MYR 268.52	MYR 0.09	MYR 283.04	MYR 0.09	MYR 235.73	MYR 0.08
4000	MYR 471.46	MYR 0.12	MYR 184.61	MYR 0.05	MYR 201.39	MYR 0.05	MYR 212.28	MYR 0.05	MYR 707.18	MYR 0.18
5000	MYR 377.16	MYR 0.08	MYR 590.74	MYR 0.12	MYR 644.45	MYR 0.13	MYR 679.30	MYR 0.14	MYR 565.75	MYR 0.11
6000	MYR 707.18	MYR 0.12	MYR 492.28	MYR 0.08	MYR 537.04	MYR 0.09	MYR 566.08	MYR 0.09	MYR 471.45	MYR 0.08
7000	MYR 606.16	MYR 0.09	MYR 421.95	MYR 0.06	MYR 460.32	MYR 0.07	MYR 485.21	MYR 0.07	MYR 404.10	MYR 0.06
8000	MYR 942.91	MYR 0.12	MYR 369.21	MYR 0.05	MYR 402.78	MYR 0.05	MYR 424.56	MYR 0.05	MYR 795.58	MYR 0.10
9000	MYR 838.14	MYR 0.09	MYR 738.42	MYR 0.08	MYR 805.56	MYR 0.09	MYR 377.39	MYR 0.04	MYR 707.18	MYR 0.08
10000	MYR 754.33	MYR 0.08	MYR 664.58	MYR 0.07	MYR 725.00	MYR 0.07	MYR 764.21	MYR 0.08	MYR 636.46	MYR 0.06
11000	MYR 1,071.49	MYR 0.10	MYR 604.16	MYR 0.05	MYR 659.09	MYR 0.06	MYR 694.73	MYR 0.06	MYR 578.60	MYR 0.05
12000	MYR 982.20	MYR 0.08	MYR 553.82	MYR 0.05	MYR 604.17	MYR 0.05	MYR 636.84	MYR 0.05	MYR 942.91	MYR 0.08
13000	MYR 906.65	MYR 0.07	MYR 908.83	MYR 0.07	MYR 557.69	MYR 0.04	MYR 587.85	MYR 0.05	MYR 870.38	MYR 0.07
14000	MYR 1,212.31	MYR 0.09	MYR 843.91	MYR 0.06	MYR 920.64	MYR 0.07	MYR 970.42	MYR 0.07	MYR 808.21	MYR 0.06
15000	MYR 1,131.49	MYR 0.08	MYR 787.65	MYR 0.05	MYR 859.26	MYR 0.06	MYR 905.73	MYR 0.06	MYR 754.33	MYR 0.05
16000	MYR 1,443.83	MYR 0.09	MYR 738.42	MYR 0.05	MYR 805.56	MYR 0.05	MYR 849.12	MYR 0.05	MYR 1,104.97	MYR 0.07
17000	MYR 1,358.90	MYR 0.08	MYR 1,085.91	MYR 0.06	MYR 758.17	MYR 0.04	MYR 799.17	MYR 0.05	MYR 1,039.97	MYR 0.06
18000	MYR 1,283.41	MYR 0.07	MYR 1,025.58	MYR 0.06	MYR 1,118.83	MYR 0.06	MYR 754.77	MYR 0.04	MYR 982.20	MYR 0.05
19000	MYR 1,588.06	MYR 0.08	MYR 971.61	MYR 0.05	MYR 1,059.95	MYR 0.06	MYR 1,117.26	MYR 0.06	MYR 930.50	MYR 0.05
20000	MYR 1,508.66	MYR 0.08	MYR 923.03	MYR 0.05	MYR 1,006.95	MYR 0.05	MYR 1,061.40	MYR 0.05	MYR 1,272.93	MYR 0.06
21000	MYR 1,436.82	MYR 0.07	MYR 1,265.86	MYR 0.06	MYR 959.00	MYR 0.05	MYR 1,010.86	MYR 0.05	MYR 1,212.31	MYR 0.06
22000	MYR 1,735.81	MYR 0.08	MYR 1,208.32	MYR 0.05	MYR 915.41	MYR 0.04	MYR 964.91	MYR 0.04	MYR 1,157.21	MYR 0.05
23000	MYR 1,660.34	MYR 0.07	MYR 1,155.79	MYR 0.05	MYR 1,260.87	MYR 0.05	MYR 1,329.06	MYR 0.06	MYR 1,506.60	MYR 0.07

Total Output	Average Cost per Chip				
276000	single-site	quad-sites	octal-sites	x16-sites	x32-sites
	MYR 0.0846	MYR 0.0612	MYR 0.0606	MYR 0.0607	MYR 0.0679

Table 8: Summary of Total Cost of the Production Output Simulation

Profit

Output	single-site	Profit per chip	quad-sites	Profit per chip	octal-sites	Profit per chip	x16-sites	Profit per chip	x32-sites	Profit per chip
1000	MYR 4,478.54	MYR 4.48	MYR 4,211.58	MYR 4.21	MYR 4,144.44	MYR 4.14	MYR 4,100.88	MYR 4.10	MYR 4,242.82	MYR 4.24
2000	MYR 9,664.27	MYR 4.83	MYR 9,530.79	MYR 4.77	MYR 9,497.22	MYR 4.75	MYR 9,475.44	MYR 4.74	MYR 9,546.41	MYR 4.77
3000	MYR 14,221.39	MYR 4.74	MYR 14,603.86	MYR 4.87	MYR 14,581.48	MYR 4.86	MYR 14,566.96	MYR 4.86	MYR 14,614.27	MYR 4.87
4000	MYR 19,328.54	MYR 4.83	MYR 19,615.39	MYR 4.90	MYR 19,598.61	MYR 4.90	MYR 19,587.72	MYR 4.90	MYR 19,092.82	MYR 4.77
5000	MYR 24,372.84	MYR 4.87	MYR 24,159.26	MYR 4.83	MYR 24,105.55	MYR 4.82	MYR 24,070.70	MYR 4.81	MYR 24,184.25	MYR 4.84
6000	MYR 28,992.82	MYR 4.83	MYR 29,207.72	MYR 4.87	MYR 29,162.96	MYR 4.86	MYR 29,133.92	MYR 4.86	MYR 29,228.55	MYR 4.87
7000	MYR 34,043.84	MYR 4.86	MYR 34,228.05	MYR 4.89	MYR 34,189.68	MYR 4.88	MYR 34,164.79	MYR 4.88	MYR 34,245.90	MYR 4.89
8000	MYR 38,657.09	MYR 4.83	MYR 39,230.79	MYR 4.90	MYR 39,197.22	MYR 4.90	MYR 39,175.44	MYR 4.90	MYR 38,804.42	MYR 4.85
9000	MYR 43,711.86	MYR 4.86	MYR 43,811.58	MYR 4.87	MYR 43,744.44	MYR 4.86	MYR 44,172.61	MYR 4.91	MYR 43,842.82	MYR 4.87
10000	MYR 48,745.67	MYR 4.87	MYR 48,835.42	MYR 4.88	MYR 48,775.00	MYR 4.88	MYR 48,735.79	MYR 4.87	MYR 48,863.54	MYR 4.89
11000	MYR 53,378.51	MYR 4.85	MYR 53,845.84	MYR 4.90	MYR 53,790.91	MYR 4.89	MYR 53,755.27	MYR 4.89	MYR 53,871.40	MYR 4.90
12000	MYR 58,417.80	MYR 4.87	MYR 58,846.18	MYR 4.90	MYR 58,795.83	MYR 4.90	MYR 58,763.16	MYR 4.90	MYR 58,457.09	MYR 4.87
13000	MYR 63,443.35	MYR 4.88	MYR 63,441.17	MYR 4.88	MYR 63,792.31	MYR 4.91	MYR 63,762.15	MYR 4.90	MYR 63,479.62	MYR 4.88
14000	MYR 68,087.69	MYR 4.86	MYR 68,456.09	MYR 4.89	MYR 68,379.36	MYR 4.88	MYR 68,329.58	MYR 4.88	MYR 68,491.79	MYR 4.89
15000	MYR 73,118.51	MYR 4.87	MYR 73,462.35	MYR 4.90	MYR 73,390.74	MYR 4.89	MYR 73,344.27	MYR 4.89	MYR 73,495.67	MYR 4.90
16000	MYR 77,756.17	MYR 4.86	MYR 78,461.58	MYR 4.90	MYR 78,394.44	MYR 4.90	MYR 78,350.88	MYR 4.90	MYR 78,095.03	MYR 4.88
17000	MYR 82,791.10	MYR 4.87	MYR 83,064.09	MYR 4.89	MYR 83,391.83	MYR 4.91	MYR 83,350.83	MYR 4.90	MYR 83,110.03	MYR 4.89
18000	MYR 87,816.59	MYR 4.88	MYR 88,074.42	MYR 4.89	MYR 87,981.17	MYR 4.89	MYR 88,345.23	MYR 4.91	MYR 88,117.80	MYR 4.90
19000	MYR 92,461.94	MYR 4.87	MYR 93,078.39	MYR 4.90	MYR 92,990.05	MYR 4.89	MYR 92,932.74	MYR 4.89	MYR 93,119.50	MYR 4.90
20000	MYR 97,491.34	MYR 4.87	MYR 98,076.97	MYR 4.90	MYR 97,993.05	MYR 4.90	MYR 97,938.60	MYR 4.90	MYR 97,727.07	MYR 4.89
21000	MYR 102,513.18	MYR 4.88	MYR 102,684.14	MYR 4.89	MYR 102,991.00	MYR 4.90	MYR 102,939.14	MYR 4.90	MYR 102,737.69	MYR 4.89
22000	MYR 107,164.19	MYR 4.87	MYR 107,691.68	MYR 4.90	MYR 107,984.59	MYR 4.91	MYR 107,935.09	MYR 4.91	MYR 107,742.79	MYR 4.90
23000	MYR 112,189.66	MYR 4.88	MYR 112,694.21	MYR 4.90	MYR 112,589.13	MYR 4.90	MYR 112,520.94	MYR 4.89	MYR 112,343.40	MYR 4.88

Total Output	Profit per Chip				
276000	single-site	quad-sites	octal-sites	x16-sites	x32-sites
	MYR 4.87	MYR 4.89	MYR 4.89	MYR 4.89	MYR 4.88
	98.29%	98.76%	98.77%	98.77%	98.63%

Table 9: Profit Summary for the Production Output

V. CONCLUSION

The validation process provides evidence that increments in the number of test sites do not necessarily result in reduction in cost-of-test and improvement of the profit margin. The case study show that increasing the number of test sites does not guarantee an improvement to throughput, cost of testing, and profit margin. The main reasons for such this scenario are presented in Figures 19 below:-

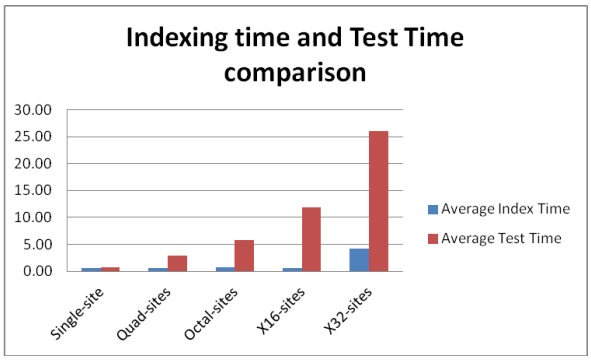

Figure 19: Comparison of the Indexing Time and Test Time for the Pick-and-Place Test equipment.

Testing throughput is the main contributor to the cost of testing and profit margin. Testing throughput is affected by the indexing time and test time. Figures 19 above show that although the indexing time for the pick and place test-equipment setup steadily increases but the test time for the test equipment increases significantly once it reaches higher test-site configuration. Therefore, the test time is the root cause of the decrease in testing speed and the reduction in testing throughput, which result in an increase in testing cost, and consequently, a decrease in profit margin.

Thus, this study concludes that simply increasing the number of test sites is not sufficient to improving testing throughput. Instead, the test time should also be reduced. The test time can be reduced in a number of ways, such as reduced pin-count testing and concurrent test among others.

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