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A UWB power divider with good isolation performance is proposed in [5], this divider is formed by installing a pair of branching in Stepped-impedance lines to two symmetrical output ports. Another different method to achieve UWB is inter- connection of two ways Wilkinson power divider is given in [2]. And other method is dividing ratio equalization of power divided combiner used in a power amplifier [3]. In this paper the structure is a planar structure, here planar structure means taken ground then substrate and at the last patch. Many structures are fabricated for power divider is based on waveguide structure [4].

many millimeter-wave systems and needed in many microwave applications such as phased antenna arrays and power amplifiers, antenna feeders, etc. Because WB technology has the characteristics of low cost, high data transmission rate, and very low power consumption, it is promising and attractive in many industrial electronic systems [9]. However, its narrow bandwidth is a serious barrier for the WB application. Among them, the wideband (WB) devices have attracted great interest in industrial communities on exploring various WB industrial electronic systems since the U.S. Federal Communications Commission released the unlicensed use of UWB (3.1-10.6 GHz) for commercial communication applications in 2002 [10]. The disadvantage of Waveguide based power divider is with an increasing number of power-dividing ports, the radius of the radial waveguide in [4] or the conical line in [6] will increase, which will cause higher order modes to be presented in the radial -waveguide or conical-line power dividing cavity due to discontinuities, and cannot be suppressed effectively, but in microstrip based power divider has not this type problem.

KEYWORDS - impedance matching, microstrip components, Power divider, power-dividing ports, wideband (WB), Wilkinson power divider, Ultra-wide band (UWB).

I. INTRODUCTION A power divider for RF power division and combination is basic passive component and applied to

ABSTRACT: A novel compact wideband (2-12 GHz) Wilkinson equal power divider on microstrip line is proposed in this paper. In this paper, a novel approach to the design of a Wideband (2-12) power divider is presented. In order to achieve the wideband performance, the divider is established by introducing variable width of microstrip line between input lines to output lines of different impedance. Finally, a compact power divider is designed, and it is demonstrated that 3 dB powers splitting from one input port to two output ports is achieved. In addition, good impedance matching at all the three ports and excellent isolation between two output ports are obtained over the specified 2-12 GHz WB range. The simulated and measured input return loss is approximately 21 dB at center frequency 7.92 GHz. The average insertion loss, and group delay are around 3 dB (including the 3-dB power-dividing insertion loss) and around 0.09 ns over across the WB. In addition, the measured and simulated isolation between the output ports is approximately 25 dB at center frequency 7.92 GHz.

Modified Wilkinson Compact Wide Band (2-12GHz) Equal **Power Divider**

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In this paper, a novel approach to the design of an Ultra-Wideband power divider is presented. In order to achieve the ultra-wideband performance, the divider is established by introducing variable width of microstrip line between input lines to output line of different impedance. Good insertion/return losses are achieved as demonstrated in simulation and measurement. In the following, the design results indicate that the proposed WB power divider has several advantages, such as wide bandwidth, large one input and two output ports (compact and simple design), excellent input impedance matching, low insertion loss, good balance of amplitude and phase at output ports, and flat group delay within the WB. It can be noted that such a structure can be utilized to a WB active power-combining system and can include large numbers of active power devices to provide high power. Obviously, this type of microstrip planar UWB power divider is different from the waveguide based power dividers [7]–[8].

II. STRUCTURE AND DESIGN OF TWO-WAY POWER DIVIDER 2.1 STRUCTURE OF PROPOSED POWER DIVIDER

Fig.1 shows the schematic diagram of the traditional two-section Wilkinson power divider with matched port. For better coupling and impedance matching, as can be seen in Fig. 2. The proposed WB power divider is simulated with commercial software CSTv11 and measured by Agilent N5230C network analyzer. The dimensions of a power divider with relative good performance were determined. The isolating resistor $R=100\Omega$. Basically here the structure is based on the method of microstrip variable width. And for improving the large bandwidth using variable width technology which is shown in Fig.2 shown the width and length of substrate. The WB power divider has simulated and measured on the FR-4 substrate with a dielectric constant of 4.01 and a thickness of 1.0 mm. and the isolator resistor R=100 Ω has used. And all dimensions are shown in TABLE 1.



Fig.1 Traditional two-way Wilkinson power divider



Fig.2 Layout of Proposed WB Power Divider (Simulated Structure on CST) (Dimension 15mm × 10.3mm)



Fig.3 fabricated Structure of Proposed WB Power Divider (Dimension is 15 mm×10.3 mm)

				Ŧ. /	
Dimension	LI	L2	L3	L4	L5
Calculated value	4.1	6.0	4.2	1.7	15
Dimension	L6	X1	X2	W	S 1
Calculated value	10.3	0.9	0.7	1.0	0.3

TABLE 1: DIMENSIONS OF THE POWER DIVIDER (UNIT: MILLIMETERS)

2.2 CIRCUIT DESIGN OF PURPOSED POWER DIVIDER

Fig.3 (a) shows a standard circuit model of two-way power divider. Here loads are represented by R_1 , R_2 and Z_{21} , Z_{22} and θ_1 for characteristic impedances and electrical lengths of the upper and lower transmission lines. The characteristic impedances and electrical lengths of additional transmission lines are denoted by Z_{22} and θ_2 .



Fig. 3(a) circuit model

2.3 EVEN-MODE ANALYSIS

We define the fed power ratio of port 3 to port 2 to be k^2 to 1. The following equation holds under the condition that the voltages at port 2 and port 3 are equal.

$$k^2 = \frac{|S_{31}|^2}{|S_{21}|^2} \tag{1}$$

When the circuit shown in Fig. 3(a) is excited by the even-mode, the circuit can be divided into two equal circuits as shown in Fig. 3(b). When the ratio of the upper circuit elements to the lower circuit elements is k^2 to 1.the two equal circuits have symmetric voltage distribution, and no currents flow to the isolation resistor [1], [11].

Therefore,

$$R_{12} = (1+k^2) R_1 \tag{2}$$

Let Y_{INb}^{eve} denote input admittance from port 2 to port 1. From the matching condition, the relationship between Y_{INb}^{eve} and terminal admittance $1/R_2$ is given by the following equation



Fig.3 (b) even mode symmetrical circuit of equivalent circuit

$$Y_{INb}^{eve} = \frac{Z_{21} + jR_{12}\tan\theta_1}{Z_{21}(R_{12} + jZ_{21}\tan\theta_1)} + j\frac{\tan\theta_2}{Z_{22}} = \frac{1}{R_2}$$
(3)

From the real part of (3)

$$\frac{Z_{22}}{Z_{21}} = -\frac{Q}{p} \tag{4}$$

and from the imaginary part,

$$1 - \frac{Z_{21}^2}{R_{12}R_2} = 1 - \frac{Z_{21}^2}{(1+k^2)R_1} = \frac{p}{(\tan\theta_1)^2}$$
(5)

where

$$P = \frac{R_{12}}{R_2} - 1 = \frac{(1+k^2)R_1}{R_2} - 1 \tag{6}$$

$$Q = (\tan \theta_1) (\tan \theta_2) \tag{7}$$

2.4 ODD-MODE ANALYSIS

When ports 2 and 3 are excited by an equal amplitude and out-of-phase current, the circuit is divided as shown in Fig. 3(c).

Therefore, we get the following equation:

$$\mathbf{k}^2 = \frac{|\mathbf{s}_{31}|^2}{|\mathbf{s}_{21}|^2} \tag{8}$$

Calculating the below circuit likewise by even-mode analysis,



Fig.3 (c) odd mode symmetrical circuit of equivalent circuit

$$Y_{IND}^{odd} = \frac{Z_{22} + jR_{x2}\tan\theta_2}{Z_{22}(R_{x2} + jZ_{22}\tan\theta_2)} + \frac{1}{jZ_{21}\tan\theta_1} = \frac{1}{R_2}$$
(9)

From the real part,

$$I - \frac{R_{X2}}{R_1} = I - \frac{(\tan \theta_2)^2}{p}$$
(10)

and from the imaginary part

$$\{\frac{Z_{22}}{Z_{21}} + Q\}R_{x2} = \frac{Z_{22}^2}{R_2}Q$$
(11)

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 $\langle \mathbf{a} \rangle$

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Solving (4), (5), (10), and (11),

$$Z_{21} = \sqrt{\frac{(1+k^2)Z_{22}^2R_1R_2}{(1+k^2)R_1R_2+Z_{22}^2(1-P)}}$$
(12)

$$R_{x2} = \frac{Z_{22} p}{(1+k^2)R_1}$$
(13)

$$\mathbf{R} = (1 + \frac{1}{k^2}) \, \mathbf{R}_{\mathbf{x}\mathbf{2}} = \frac{\mathbf{Z}_{\mathbf{2}\mathbf{2}}^2 \, \mathbf{p}}{k^2 \, \mathbf{R}_1} \tag{14}$$

$$\theta_{1} = \tan^{-1} \left[\pm \sqrt{\left\{ \frac{(1+k^{2})R_{1}R_{2}p}{(1+k^{2})R_{1}R_{2}-Z_{21}^{2}} \right\}} \right]$$
(15)

$$\theta_{2} = \tan^{-1} \left[\pm \sqrt{P\{1 - \frac{Z_{22}^{2}p}{(1+k^{2})R_{1}R_{2}}\}} \right]$$

$$= \tan^{-1} \left[\pm \sqrt{P\{1 - \frac{Z_{22}^2 P}{(1+k^2)R_1R_2}\}} \right]$$
(16)

Equation (6) must be positive from (14) and (16). Therefore

$$\frac{R_2}{R_1} < 1 + k^2 \tag{17}$$

Since the above equations are incomplete, one parameter needs to be determined to determine all of the circuit parameters. If the sign of (15) is negative, the sign of (16) must be positive by (4) and (7). Regarding the ranges of all values, firstly, (15) gives the ranges of Z_{21} and θ_1 , and, secondly, (15) gives the range of Z_{22} . Finally the ranges of θ_2 and R are determined. Consequently,

$$\sqrt{(1+k^2)R_1R_2} \ge Z_{21} > 0 \tag{18}$$

$$\sqrt{\frac{(1+k^2)R_1R_2}{p}} \ge Z_{22} > 0 \tag{19}$$

$$(1+k^{-2})R_1 \ge R > 0$$
 (20)

$$\pi (n+1) - \tan^{-1} \sqrt{P} > \theta_1 \ge n\pi + \frac{\pi}{2}$$

$$\tag{21}$$

$$m\pi + \tan^{-1}\sqrt{P} > \theta_2 \ge m\pi \tag{22}$$

Where n and m are any integer

Once one of these parameters is given within these ranges, all other values are determined. If k^2 and $R_1 = R_2 = 1$, the above expressions are the same as the expressions presented by Horst [12].

III. SIMULATION AND RESULTS

Fig.6 shows the simulated and measured results of the designed WB power divider. Fig.6 as can be seen in this graph, the input power has been split equally to the two output ports. The isolation is less than -10 dB, and the two insertion loss and the return loss show the excellent performance over the WB band Very good input port matching is achieved with S11, simulated -21.2 dB and measured -21 at the design frequency (7.92 GHz) as shown in Fig. 6, and the agreement between both full-wave simulators can be clearly seen. Fig.7 (a) shows that the transmission parameters (S21and S31) are very close to their theoretical values of simulated 3 dB and measured -2.91 dB at the design WB, which shows the equal-split behavior of this divider. The small discrepancies could be due to losses and discontinuities. Fig. 8 shows the isolation between the 2-way power divider output ports. As mentioned before, the isolation between the output ports at the design frequency (7.92 GHz) is as good as that in the Wilkinson power divider. From Fig.8, it can be seen that S23 equal to simulated -25.2 dB and measured -24.28 at design frequency 7.92 GHz, while it is noted that the best isolation seems to be between ports 2 and 3 less than -10 dB at the WB. Fig.5 shows the output ports matching, Parameters S22 and S33, WB power divider. As mentioned in the introduction, the output ports are matched at the design frequency, and according to Fig. 5, the output ports return losses are all less than -10 dB at the design frequency (7.92 GHz). In addition, the simulated group delays show good linearity within WB, as shown in Fig. 9. The mean of flat group delay is the signal from input port to output ports reach at same time so there is no delay. Here at WB

the total group delay is 0.09 ns which is very negligible group delay between output signals. All simulated and measured results are shows in TABLE 2.

S. No.	Freq. Band (GHz)	Reso- nant Freq. (GHz)	Isolation (dB)		Return Loss (dB)		Group delay (ns)	Insertion loss (dB)	
			Simulated	Measured	Simulated	Measured	Simulated	Simulated	Measured
1	2-12	7.92	25.2	24.28	\$11=21.2 \$22=17.85 \$33=17.82	\$11=21 \$22=18.2 \$33=18.4	0.090	3	2.91

TABLE 2: SIMULATED AND MEASURED RESULTS OF WIDE-BAND POWER DIVIDER



Fig.4 Return loss of Proposed Power Divider



Fig.5 Return loss at output ports (n=2, 3)



Fig.6 Simulated and measured result of the proposed power divider





(b)

Fig.7 Simulated Transmission coefficients of WB power divider (n = 2, 3). (a) Amplitude. (b) Insertion Phase

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Fig.8 Isolation between output ports



Fig. 9 Simulated and measured group delays of the proposed power divider

IV. CONCLUSION

In this paper, a unique method of designing an ultra-wideband (WB) equal power divider using the divider is established by introducing variable width of microstrip line between input lines to output line of different impedance on microstrip line is proposed. Through the simulation, good power splitting, impedance matching and isolation can be obtained. The structure occupies an area of $15\text{mm} \times 10.3 \text{ mm}$. The circuit integration is enhanced because of the special placement of the isolation elements. Simulated and measured results show that it makes the 3 dB power divider work preferably in a wide bandwidth. All simulated and measured result matched by measured result. It is proven by calculation that the response of the dividers is symmetrical about the center frequency.

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