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Performance Analysis of A Driver Cricuit and An Input Amplifier for BCC

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Abstract: - Body-Coupled Communication (BCC) is based on the principle of electrical field data transmission attributable to capacitive coupling through the human body. In this paper, we have newly proposed a voltage mode driver circuit in the transmitter (Tx) part and an input amplifier in the receiver (Rx) part to construct a transceiver for (BCC). The entire work is designed in ST65 nm CMOS technology. The driver circuit is cascaded of two single-stage inverter and an identical inverter with drain resistor. The cycle to cycle jitter is 0.87% which is well below to the maximum point and the power supply rejection ratio (PSRR) is 65 dB indicating the good emission of supply noise. A flipped voltage follower (FVF) topology is used for designing the input amplifier to support the low supply voltage. The open loop gain is 24.01 dB and the close loop gain is 19.43 dB for this amplifier. The performance analysis is evaluated on the basis of corner analysis, noise analysis and eye diagram to find out the best possible results. The total system is maintained with very low supply voltage of 1-1.2V.

Keywords: - *BCC, FVF, driver cirtuit, amplifier, corner analysis, eye diagram*

I. INTRODUCTION

Body-Coupled Communication (BCC) is one of the most interesting topics in the recent years. Communication through the body is attractive to the researchers due to its low power operation. BCC is clearly defined by Body Area Network (BAN). BAN is formally defined by IEEE 802.15 as "A communication standard optimized for low power devices and operation on, in or around the human body (but not limited to humans) to serve a variety of applications, including medical, consumer electronics, personal entertainment and other" [1].

The strongest motivation of using human body as a communication channel is its speed, less interference, low power consumption and inherent security system compared with the existing wireless communication systems like Bluetooth, Zigbee and WiFi. The low power transceiver for BAN is mainly focused on developing an architecture of transceiver using human body as a communication channel that is capable of higher data rate (10 Mbs) operating at 10 MHz frequency range. This application of near field communication (NFC) with BAN is going to increase the number of application as well as solves the problem with cell based communication system depending upon the frequency allocation. So the inductive or capacitive coupling technique by using a human body as a communication channel could be a solution for the wireless or mobile communication system. Moreover, a low power transceiver for BAN would be given in favor of capacitive coupling as viable means of next generation touch-and-go communication.

BCC can operate at MHz frequencies without large couplings because the signals transmit between the conductive human tissues of the body coupled transceiver and the floated ground with a capacitive return path [2]. Basically, Low impedance capacitive coupling consumes most of the power. So, it is possible to reduce the power consumption by using a low impedance capacitive coupling. This communication system has different applications such as human health monitoring system, cardiac monitoring, blood pressure measuring, business card handshake and door code unlock.

This paper presents a driver circuit for the transmitter (Tx) and an input amplifier for receiver (Rx) to support the BCC. In figure 1, the overall idea behind the entire work is illustrated. It is a half duplex communication system that the digital data is delivered by the digital transceiver (TxRx) Baseband and first

Analog Front End (AFE) TxRx receives the data. The data are transmitted by the first TxRx and it is passed through the human body with high attenuation due to high impedance provided by the human body. The attenuated signal is amplified as well as provides the digital data by the second TxRx and finally it goes back to digital TxRx baseband. The human body acts as a communication channel and it provides almost 60 dB attenuation.

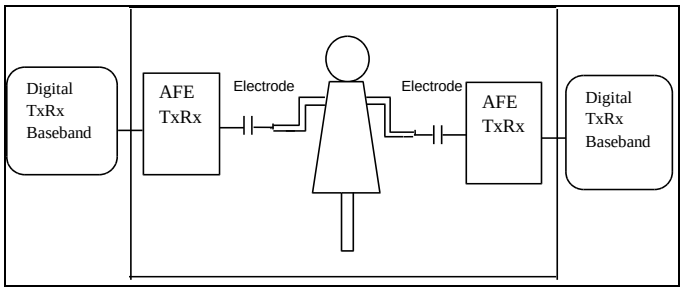

Figure 1: System description of BCC

The transmitter of the analog front end (AFE) is mainly focused on the output driver which provides ones and zeros to one side of the capacitor. It is important to maintain the shape of the signal on the other side of the capacitor by controlling the rising and falling edge of the signal. However, the attenuation factor due to high impedance provided by the human channel, the filter is not mandatory as the amplitude of the signal is very low and very minor change to get mixed with noise. On the other hand, an input amplifier of the receiver is considered to be a most complex and challenging part of the entire work. Weak signals from the transmitter need to be stronger and also need to be free from noise. Therefore, it requires an amplifier that can amplify the signal to the desired level. In this paper, a differential amplifier is designed based on the FVF topology that can give higher gain as well as low noise and low power consumption. By cascading the amplifier it is possible to obtain the higher gain. At the analog or digital interface, a Schmitt trigger is used to detect the correct information as well as low noise.

II. CHANNEL DESCRIPTION

The capacitive coupling approach is chosen for BAN because of the some physical and application advantages. Nowadays the communication demands more flexibility, security, high data rate, low power consumption, small chip area and so on. The capacitive coupling approach is the new generation touch- and-go communication system where the modeling of the human body is a challenge to characterize the channel. In figure 2, it shows the top view of the capacitively coupled human body with two electrodes.

The top view of the body model for BAN clearly shows there is no need of direct contact between the electrodes and the person. On the other hand, it is important to consider the distance as the movement of the body affects the signal on the receiver side. As the body distance is considered 2 meter or less than that so the transmitted signal should be strong enough to recover when it detects from the receiver electrodes.

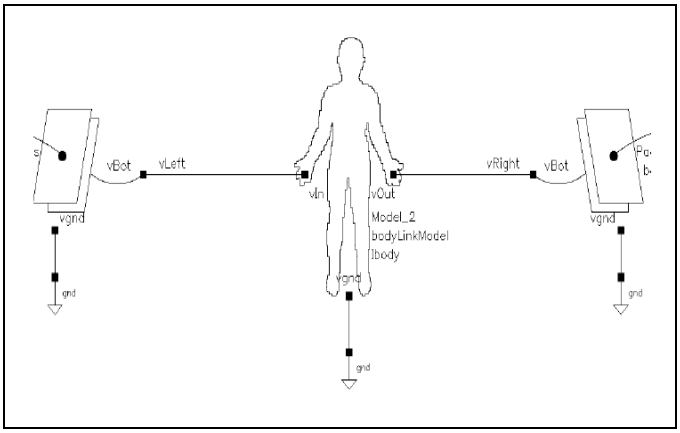

Figure 2: Body model with capacitive coupling

The receiver needs to be very sensitive enough to detect the transmitted signal as the signal is attenuated by human body. The transmission behavior of the human channel is fully depended upon the body resistance and coupling capacitor.

III. DRIVER CIRCUIT

A good driver circuit is characterized by an optimized output impedance, a controlled falling and rising edges of the signal in order to shape the pulses and of course the offset error free clean signal levels. The basic requirements of designing a strong driver circuit for BCC is to produce a significant amount of current due to high attenuation of the human body at the same time low capacitance (small plates) at the transmitter side. On the other hand, the receiver might not detect the weak signal so that the driver circuit need to maintain the voltage level. Basically, there is no filter block for this design because of very well noise reduction by the body channel which is a great advantage of BCC. In this paper, the driver circuit is designed in such a way that it can maintain the signal quality which depends on the pulse distortion, skew and systematic jitter.

In the Body-Coupled Communication project, the Manchester coded signals is chosen as it is a promising and simple modulation technique. In general, the Manchester encoding is applied to a simple transmitter consisting of only driver (inverter) driving a capacitive plate connected to the human body. Another advantage of Manchester encoding is that it is easier to integrate in hardware. However, depending on transmission modes the driver circuit divided into two basic types such as voltage mode driver and current mode driver. In this work a three stage voltage mode driver is used for measuring the leakage power consumption when the circuit is off state [3]. This architecture has very low output impedance that allows resistive region by using the CMOS technology. So it is essential to understand the basic properties of the COMS inverter. The static CMOS inverter has some important design matrix such as cost in respect to the area, integrity and robustness on the basis of static behaviour, performance analysis with the help of dynamic behaviour and the energy efficiency measured by the energy and power consumption [4].

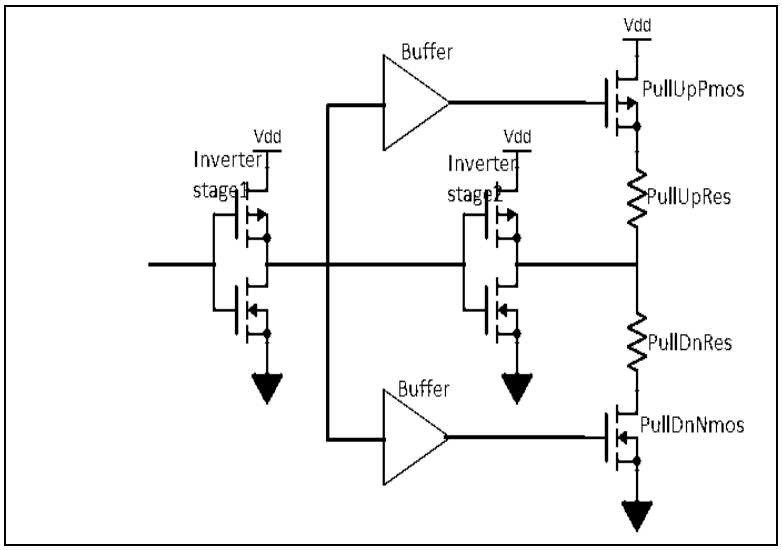

Figure 3: Basic architecture of the tri-state voltage mode driver

Table 1: Sizing technique of the transistors in the driver chain

Inverter stage	Width (NMOS)	Value (µm)	Width (PMOS)	Value (µm)
Stage 1	$W_{nStage1}$	119	3* $W_{nStage1}$	357
Stage 2	2* $W_{nStage1}$	238	3*2* $W_{nStage1}$	714
Stage 3	3* $W_{nStage1}$	476	3*2*2*$W_{nStage1}$	1428

The driver circuit demands big transistor size as the design requires high current. It is obvious that increasing the size of the transistor also increases the power consumption. It is cascaded in three stage inverters as shown in the figure 3. In table 1, it is shown that the width of the PMOS is three times with the NMOS of the same inverter. On the other hand, the width of the NMOS is two times with the preceding stage NMOS. Apart from, 195 nm length of the transistor provides proper pulses at the transmitter.

Finally, the power consumption is determined 7.398 mW for transistor level which is quite high as it is inversely proportional to the transistor width. In table 2, the power supply rejection is found 65 dB which

indicates a good emission of supply noise. The cycle to cycle jitter is lower than 1%. In addition, it consumes only 1.954 µW leakage power when the driver is in high impedance state.

Table 2: The performance of the entire driver circuit

Parameters	Value
Supply Voltage	1.2 V
Operating frequency	10 MHz
Power Consumption	7.398 mW
Propagation delay	6.14 ns
Jitter	0.87%
PSRR	65dB
Leakage power	1.954 µW

IV. AN INPUT AMPLIFIER

Depending upon the reduction of the supply power, different techniques are proposed to meet the requirement in analog and mixed signal circuits like folding, triode-mode and subthreshold operation of metal oxide semiconductor (MOS) transistors, floating gate techniques and current mode processing [5]. To maintain the requirement of the integrated circuit design, flipped voltage follower (FVF) is chosen in this work. It is a kind of basic cell, which is suitable for low power and low voltage operation. Compare to other topologies, FVF gives a wide range of frequency band and lower output impedance, which is the main advantage of this topology. It is one kind of voltage follower but the main difference of the traditional voltage follower and FVF is that FVF has low output resistance. In traditional voltage follower for improving its high output resistance, there needs to increase the transconductance gain, g_m which requires large current biasing and also the large W/L ratio.

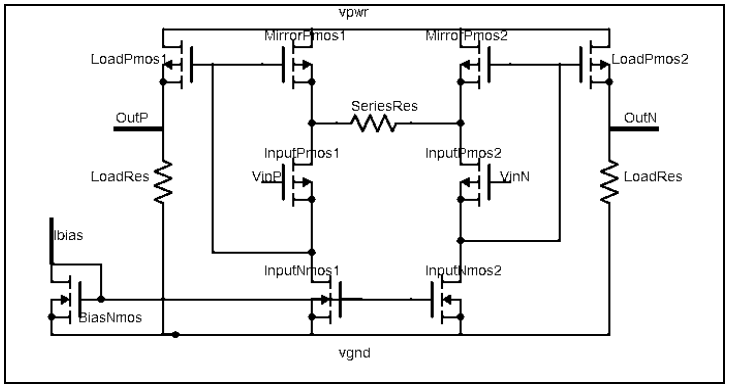

Figure 4: The transistor level implementation of an amplifier

In figure 4, the transistor level implementation of preamplifier is mentioned. The circuit is developed with the concept of flipped voltage follower. Two cascaded flipped voltage follower stages connect with a series resistance ($R_{SeriesRes}$). This resistance is mainly a degeneration resistance. The advantage of using this degeneration resistance is that when the input signal is weak, small $R_{SeriesRes}$ gives high gain and low noise. Neglecting the short-channel effect and body effect, and assuming $R_{SeriesRes} \gg 2/(g_{m1}r_{o1}r_{o2})$ [6], the equivalent input transconductance is $1/R_{SeriesRes}$ [6]. The gain of the circuit is approximately,

$$A_v \approx R_{LoadRes} / R_{SeriesRes} \qquad (1)$$

The important thing is that the gain does not depend on the transistor but they depend on the resistance. For this, it gives good linearity and high accuracy performance. The circuit is also suitable for low power like 1 V or less. In Figure 5 and 6, the open and close loop gain of the input amplifier is shown. In table 3, the overall performance of the input amplifier is mentioned.

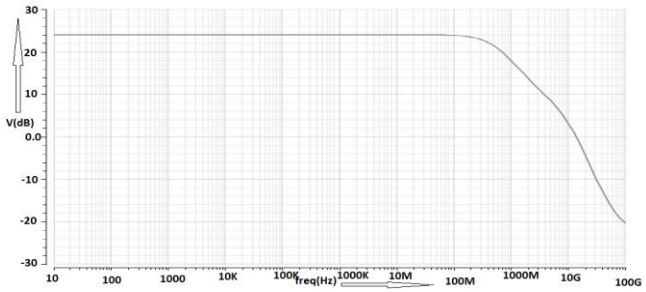

Figure 5: Open loop gain of the amplifier

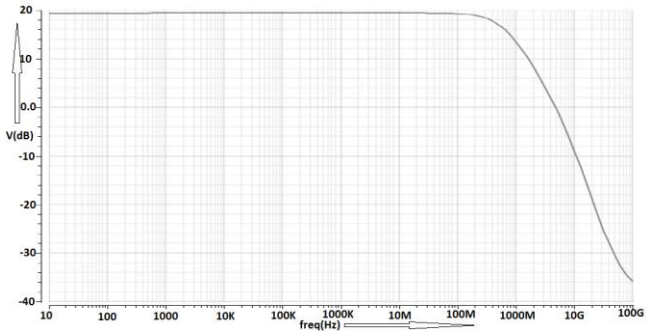

Figure 6: Close loop gain of the amplifier

Table 3: Performance analysis of the amplifier

Parameters	Value
Supply voltage	1 V
Open loop gain	24.01 dB
Close loop gain	19.63 dB
Unity-gain frequency	474 MHz
Input referred noise PSD @ 10 MHz	8.69 nV/ sqrt(Hz)
Phase margin	59.87
Power consumption	2.3 mW
Biasing current	83.931 µA

V. SIMULATION RESULTS

A. *Corner Analysis*

The corner analysis is nothing but the variation of different process nodes with different supply voltages and temperatures. For finding the worst-case performance in the integrated circuit, corner analysis gives a better view of the variations. For example, when the transistors changes their states from one logic state to another at the same time speed may change.

Figure 7 & 8 describe the corner analysis of the Tx and Rx. For Tx, the supply voltage varies from 1 V to 1.4 V but for Rx, it varies only from 0.9 V to 1.1 V. Temperature varies for the both from -40°C to 120°C. The simulation is run for 9 process corners. So the corner analysis is run for in total 9*3*3=81 points where 3 for supply voltage variation and another 3 for temperature variation.

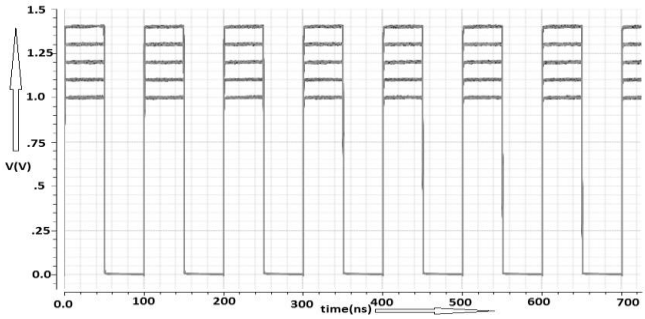

Figure 7: Corner analysis of the driver circuit

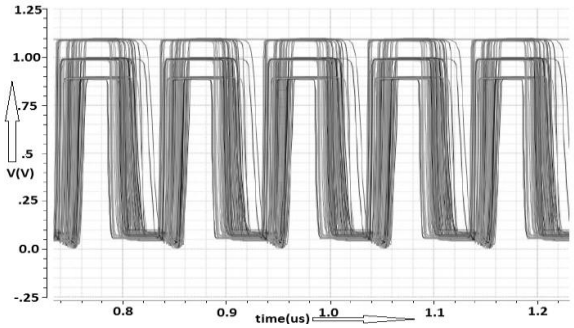

Figure 8: Corner analysis of the receive chain by using the suggested amplifier

The ones or zeros are decoded in the baseband by sampling the obtained data from the AFE. The sampling frequency is eight times of the clock frequency. From this, it is clear that one can detect when the length is more than 0.0125 µs. The length of ones and zeros are respectively 0.05 µs and 0.05 µs. From the corner analysis, it is clear that the minimum length of ones is 0.049 µs in Tx and 0.025 µs in Rx, which can be easily detected by the digital baseband.

*B. **Eye Diagram***

The eye diagram is a kind of graphical representation that can give a set of information about the high speed digital data transmission. In addition, it can give information about the noise, jitter, rise time and fall time.

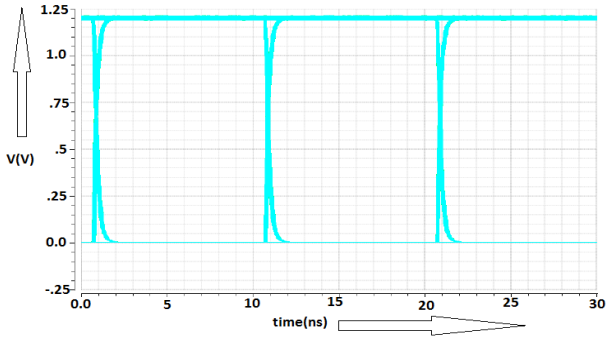

Figure 9: Eye diagram for the driver circuit performing in a Tx

In figure 9, the eye diagram for transmitted signal is presented where the simulation run for 30 ns with 10 mV supply noise. In table 4, the two basic characteristics of the eye diagram are determined that one is horizontal eye opening at 2.5 ns and another is vertical eye opening at 1.1 V. The timing variation at zero crossing indicates the amount of noise where the zero crossing occurs. The timing variation at zero crossing is measured as 0.55 ns. The cycle to cycle jitter with respect to the data clock is 0.87%.

Table 4: The results show the performance of the eye diagram in Tx

Vertical eye opening	1.1 V
Horizontal eye opening	2.5 ns
Noise margin	0.25 V
Timing variation at zero crossing	0.55 ns
Eye level zero	5 mV
Eye level one	10 mV
Rise time	1.2 ns
Fall time	1.5 ns
Jitter	0.87%

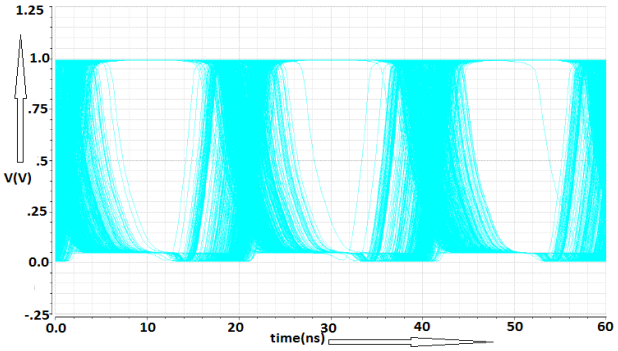

Figure 10: Eye diagram for the receiver chain

In figure 10, the eye diagram is run for 60 ns period. From the table 5, the value of horizontal eye opening is 19.5 ns and the vertical eye opening is 0.94 V. The value of timing variation of zero crossing measures at 4 ns. Noise margin is the minimum tolerance level of the proper operation of the circuit which is 0.47 V.

Table 5: Measurement table for eye diagram in Rx

Vertical eye opening	0.94 V
Horizontal eye opening	19.5 ns
Noise margin	0.47 V
Timing variation at zero crossing	4 ns
Eye level zero	7 mV
Eye level one	1 mV
Rise time	3 ns
Fall time	4.5 ns

C. Noise Analysis

Noise is an important consideration of designing any integrated circuit because it distorts the original signal so that the detection is hampered at the receiver. Figure 11 shows the results of transmitter after adding 3 mV noise to the supply voltage. Figure 12 shows the noise performance after adding 1 mV noise to the supply. Signal is recovered successfully by passing it through the input amplifier. It is not possible to recover the original signal if the noise is more than 2 mV in the Rx.

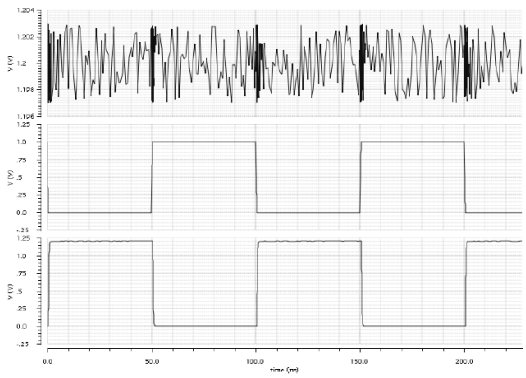

Figure 11: The waveform of the input data and the transmitter output by adding 3 mV noise

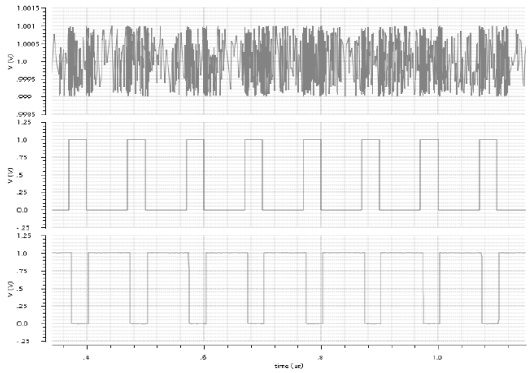

Figure 12: Adding 1mV noise to the supply voltage and showing output signal of Tx, Rx

VI. CONCLUSION

In BCC application, the proposed driver circuit gives progressive value in terms of jitter calculation, power leakage and also in PSRR compare to other circuit. The proposed input amplifier for Rx has provided some noteworthy results in gain performance, noise and power consumption. It is very difficult to maintain a low noise and low power consumption in low supply voltage but this architecture provides the improvement value of 8.69 nV/sqrt(Hz) and 2.3 mW respectively. We also highlighted the construction and function of the human body channel. Finally, this work can be considered as a new gateway for future improvement of BCC.

VII. ACKNOWLEDGMENT

It was very challenging for us at the beginning to adopt the overall system but we are very thankful to our teachers, seniors and friends to make a successful completion of this work.

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