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Investigation of Total Harmonic Distortion (THD) for the Optimize Design of a Single-Phase Seven-Level Diode Clamped Multi-Level Inverter

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ABSTRACT
In this paper the Investigation of Total Harmonic Distortion (THD) for the Optimize Design of a Single-phase seven-level Diode Clamped Multilevel Inverter is implemented. The THD analysis of the single-phase seven-level diode clamp multi-level inverter is performed using phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) SPWM switching control techniques at varying modulation index (m_i) of 0.6 to 1.0. The result obtained from MATLAB/SIMULINK simulation for THD of the DCMLI using PD SPWM for modulation index of 0.6 to 1.0 shows that the APOD SPWM has the lowest THD of 17.89 % at a modulation index of 1.0.
Keywords *– Alternate phase opposition disposition (APOD), Phase disposition (PD), Phase opposition disposition (POD), Pulse width modulation (PWM), Total harmonic distortion (THD*

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I. INTRODUCTION

The process through which the Inverter converts DC power supply to AC power supply is called inversion. This inversion process is the reverse of the rectifier process, where the AC supply is converted into DC power supply.

The input voltage, output voltage and frequency of an inverter depend on the design of the circuit. A power inverter can be entirely electronics or may be a combination of mechanical effects and electronic circuit [1]

Multi-level converters (MLCs) offer several advantages in terms of high power capability, transformer less operation, short-circuit protection, and excellent quality of output current waveform [2]

There are different types of power converters which include: DC-DC converters (chopper), DC-AC converters (inverters), AC-DC converters (rectifiers) and AC-AC converters (converter) [3]. Converters can come in many different varieties, differing in price, power, efficiency and purpose. Recently, converters have become more and more common over the past several years as support for self-sufficient power has increased [4].

Multilevel power conversion is used to provide more than two voltage level to achieve smoother and less distorted dc to ac power conversion and it can generate multiple step voltage waveform with less distortion, less switching frequency and higher efficiency.

Multi-Level Inverter (MLI) topologies have been widely used in the motor drive industry to run induction machines for high power and high voltage configurations [5].

MLI's divide the main dc supply voltage into several dc sources which are used to synthesize an AC voltage into a stepped approximation of the desired sinusoidal waveform. The stepped approximation is also popularly known as the staircase model (Tolbert et al.,1999). The number of stages (cells or capacitors depending on the respective topology) helps decide the power capacity of the inverter as a whole. Suitable connections either in series or shunt mode or both are done to achieve higher voltage and/or current ratings.

Multi-level converters (MLCs) offer several advantages in terms of high power capability, transformer-less operation, short-circuit protection, and excellent quality of output current waveform [2].

1.1 Multi-Level Inverters

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II. DESIGN AND ANALYSIS

2.1 System Block Diagram

Fig. 1 shows the block diagram of a single phase seven level Diode Clamp multi-level inverter. The battery bank array generates the required DC voltage of $220V_{dc}$ that the boost converter steps up to $630V_{dc}$ which is controlled by PI controller for error handling. The step up voltage is fed into a single phase seven level Diode Clamp MLI using optimized SPWM to generate switching pulses for the inverter switches which produce a seven level output voltage of $220V_{ac}$ for household load consumption.

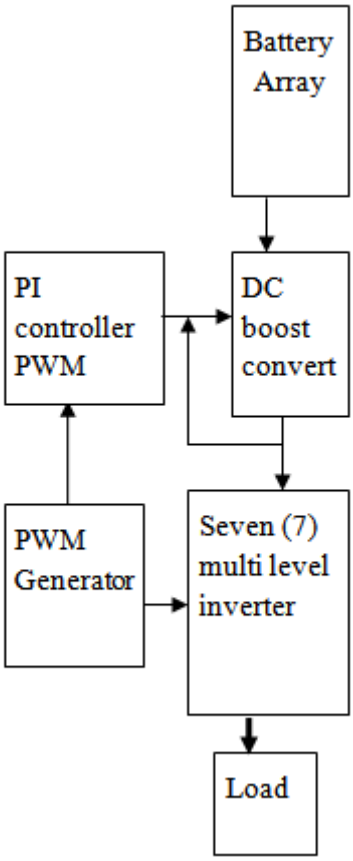

Figure 1: The block diagram of the single phase seven level Diode Clamp inverter.

2.2 Circuit Configuration and Operational Principle

The circuit in Fig. 2 shows a single phase five level DCMLI which uses twelve (12) power semiconductor switches, six (6) (n-1) where n=7, DC link capacitors and ten (10) clamping diodes. This DCMLI consists of six switching pairs (S_1, S_7), (S_2, S_8), (S_3, S_9), (S_4, S_{10}), (S_5, S_{11}) and (S_6, S_{12}). If one switch of the pair is switched on, the other complementary switch of same pair must be off. The DC-link capacitors together with the diodes clamp the switching voltage to half level of the DC bus voltage while the neutral (N) is the reference

point of the circuit. Typical switch combinations to obtain the required output voltage levels for seven-level DCMLI are as shown in Table 1.

In the circuit configuration of the single phase seven level DCMLI, each inverter phase is powered by a single DC source. With the appropriate switching of the semi-conductor switches in the modules, each of the phases produces seven output voltage levels. The switching patterns for the different voltage levels are as presented in Table 1.

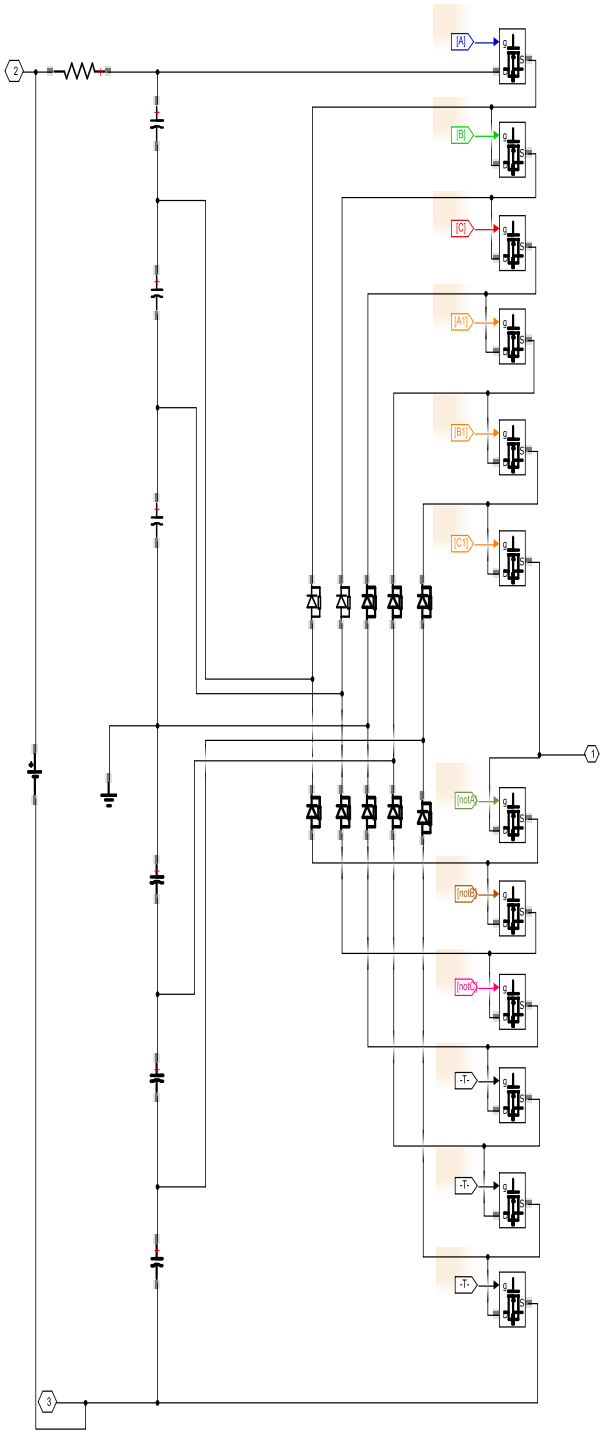

Figure 2: Single-phase Seven-Level Diode Clamped MLI

Table 1: Switching states of a Seven-level DC MLI

Output Voltage Level	Switching States											
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0
Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

III. DESIGN OF INVERTER CONTROL CIRCUIT

The Modeling of Switching Logic Equations

The operation of a traditional single-phase seven level diode clamped inverter requires six carrier ($n-1=7-1=6$) signals and a single modulating waveform. These signals combine to produce pulses for the switching of the twelve inverter switches. The analysis of the combination of the signals is as follows [7].

G is the modulating signal $m(t)$, A is the pulse obtained when the modulating signal $m(t)$ and the carrier signal $r_1(t)$ with [10 12] output values are compared, A_1 is the pulse produced when $m(t)$ and $r_2(t)$ with [8 10] output values are compared, A_2 is the resulting pulse when $m(t)$ and $r_3(t)$ with output values [6 8] are compared, B pulse results when $m(t)$ and $r_4(t)$ with [4 6] output values are compared, when $m(t)$ and $r_5(t)$ [2 4] are compared B_1 pulse is produced ,B_2 is the pulse obtained by comparing $m(t)$ and $r_6(t)$ with [0 2] values. The combination of these pulses trigger the switches numbered from S_1 to S_{12}.

The equations developed from the analysis of the signals are given by equations (24) to (35). [7]

$$S_1 = A.\overline{G} + \overline{A}.G \quad (24)$$
$$S_4 = A.G + \overline{A}.\overline{G} \quad (25)$$
$$S_5 = A_1.\overline{G} + \overline{A}_1.G \quad (26)$$
$$S_8 = A_1.G + \overline{A}_1.\overline{G} \quad (27)$$
$$S_9 = A_2.\overline{G} + A_2.G \quad (28)$$
$$S_{12} = A_2.G + \overline{A}_2.\overline{G} \quad (29)$$
$$S_3 = B.\overline{G} + \overline{B}.G \quad (30)$$
$$S_2 = B.G + \overline{B}.\overline{G} \quad (31)$$
$$S_7 = B_1.\overline{G} + \overline{B}_1.G \quad (32)$$
$$S_6 = B_1.G + \overline{B}_1.\overline{G} \quad (33)$$
$$S_{11} = B_2.\overline{G} + B_2.G \quad (34)$$
$$S_{10} = B_2.G + \overline{B}_2.\overline{G} \quad (35)$$

The modulation circuit for the single-phase of the inverter is designed using De Morgan's laws as shown in equations (36) to (47).

$$S_1 = A \oplus G \quad (36)$$
$$S_4 = \overline{A \oplus G} \quad (37)$$
$$S_5 = A_1 \oplus G \quad (38)$$
$$S_8 = \overline{A_1 \oplus G} \quad (39)$$
$$S_9 = A_2 \oplus G \quad (40)$$
$$S_{12} = \overline{A_2 \oplus G} \quad (41)$$
$$S_3 = B \oplus G \quad (42)$$
$$S_2 = \overline{B \oplus G} \quad (43)$$
$$S_7 = B_1 \oplus G \quad (44)$$
$$S_6 = \overline{B_1 \oplus G} \quad (45)$$
$$S_{11} = B_2 \oplus G \quad (46)$$
$$S_{10} = \overline{B_2 \oplus G} \quad (47)$$

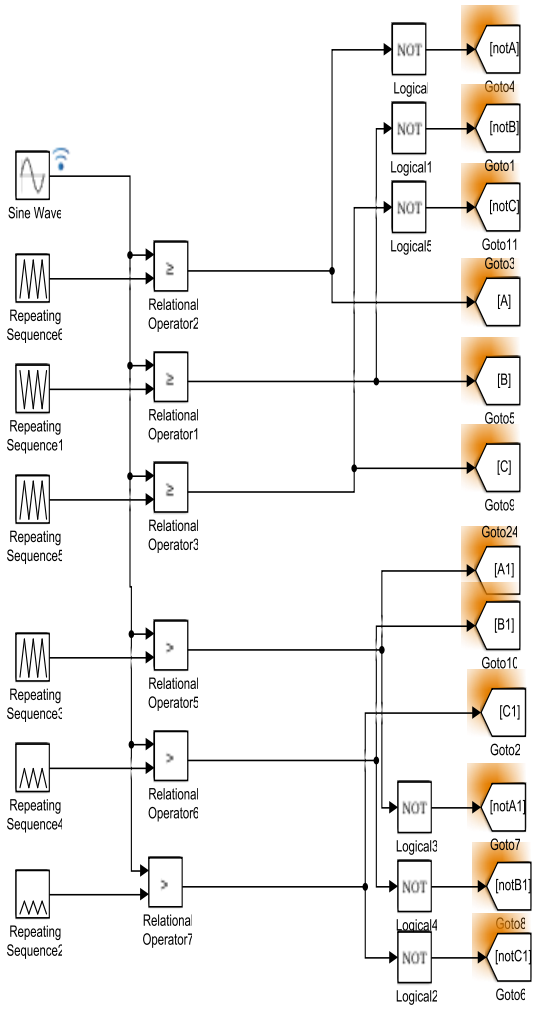

Figure 3: Sinusoidal reference and triangular carrier waves of APOD SPWM for gating pulses

IV. THD SIMULATION OF THE SINGLE-PHASE SEVEN LEVEL DCMLI FOR PD, POD AND APOD AT M.I = 0.6 TO 1.0 USING MATLAB/SIMULINK

The THD for the DCMLI was simulated for PD, POD and APOD SPWM techniques at varying modulation index of 0.6 to 1.0. The waveforms are as presented in Fig. 4 to Fig. 7.

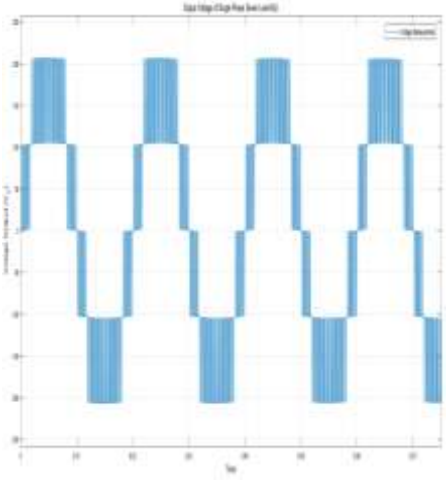

Figure 4: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.1 to 0.7 for POD PWM

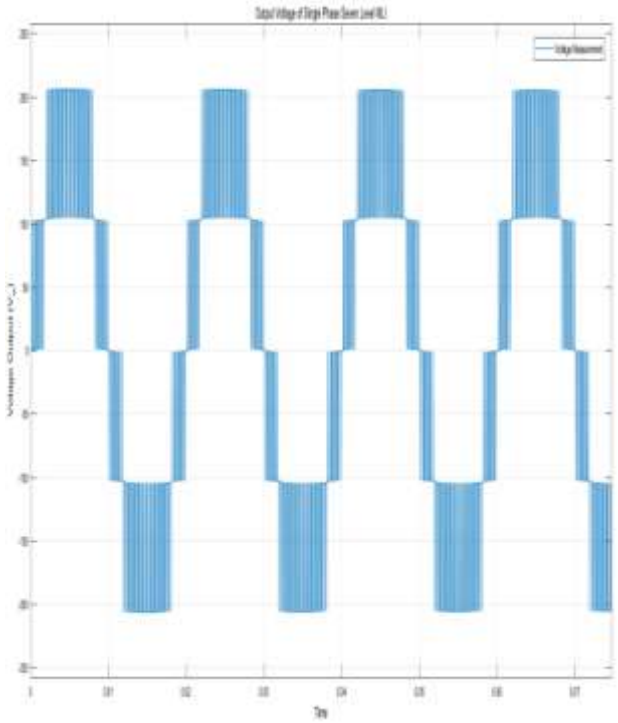

Figure 5: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.6 for PD PWM

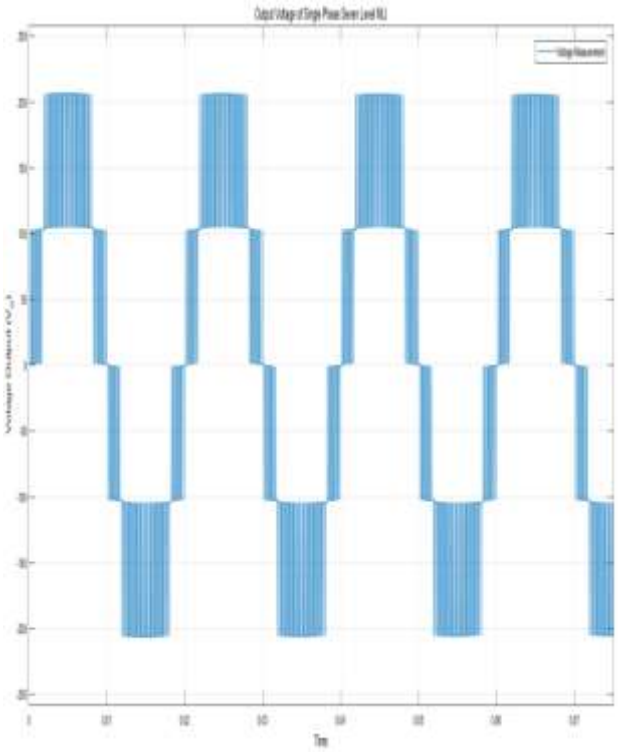

Figure 6: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.6 for POD PWM

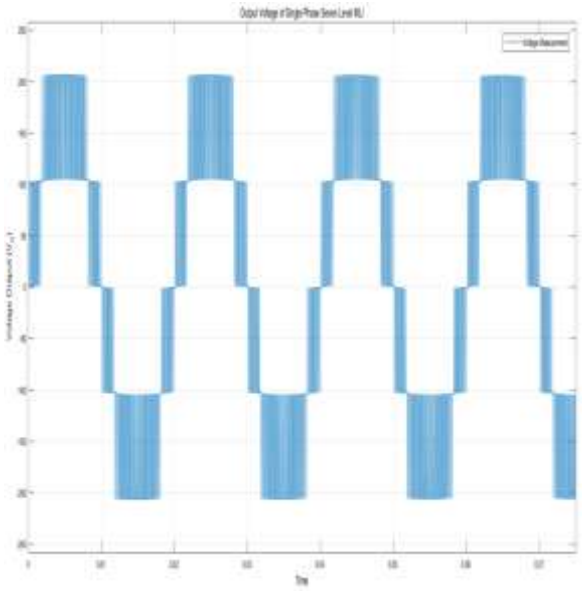

Figure 7: Voltage Output of a Single Phase Seven-Level DCMLI on no load at m=0.6 for APOD PWM

4.1 THD simulation of the single phase seven level DCMLI for PD, POD and APOD at M.I = 0.6 to 1.0 using MATLAB/SIMULINK

The results analysis from frequency of PD, POD and APOD are summarized in Table 2 to Table 4.

Table 2: THD and Fundamental magnitude of PD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag (50Hz)	Total Harmonic Distortion (THD) %
1	311.2	17.93
0.9	280.2	22.11
0.8	249.1	23.97
0.7	217.4	24.86
0.6	186.1	32.88

Table 3: THD and Fundamental magnitude of POD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50 Hz)	Total Harmonic Distortion (THD) %
1	311.2	17.92
0.9	280.2	22.09
0.8	249.1	23.96
0.7	217.4	24.84
0.6	186.1	32.86

Table 4: THD and Fundamental magnitude of APOD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50Hz)	Total Harmonic Distortion (THD) %
1	311.2	17.89
0.9	280.2	22.12
0.8	249.1	23.97
0.7	217.4	24.85
0.6	186.1	32.82

From Table 2 to Table 4, it shows that the modulation index of 1.0 has the lowest THD values of 17.93 %, 17.92 % and 17.89 % respectively with fundamental frequency amplitudes of 311.2 for PD, POD and APOD SPWM in the FFT analysis of the single phase seven level DC MLI. From table 6, it shows that APOD SPWM techniques has better THD performance than PD and POD in a single phase seven level DCMLI due to low

THD percentage recorded as 17.89 % with a magnitude of 311.2 over 3 cycles at a fundamental frequency of 50Hz over a maximum frequency of 1kHz.

V. CONCLUSION

In this work, a design and development of a Single-phase Seven-level Diode Clamped MLI using APOD SPWM technique has been achieved. The output of the inverter was observed to be 221.9V RMS with a THD of 17.89 % without filtering on no load which can be used at homes.

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