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Performance Analysis of Three-phase Seven-level Asymmetric Cascaded H-Bridge Multilevel Inverter with Reduced Number of Switches

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ABSTRACT: *Conventional cascaded multilevel inverter topologies exhibit a number of undesirable shortfalls such as low efficiency, increase in circuit complexity, high cost, high total harmonic distortion (THD) and high switching losses. This informed the basis of proposing a more reliable cascaded H-bridge multilevel inverter with reduced number of switches which is capable of mitigating these shortfalls. In this paper, MLI simulated in MATLAB has the number of switches and DC power sources reduced to eighteen and six respectively. The APOD, PD and POD carrier signals were applied to the MLI and the power quality measurements were compared. From the simulated results, the least THD was obtained at the modulation index of 1.0 and the corresponding THD values for APOD, PD and POD were 22.22%, 22.10% and 22.09% respectively. The highest THD was obtained at modulation index of 0.2 and the corresponding THD values for APOD, PD and POD were 76.98%, 79.58% and 76.98%respectively. Also the highest output voltage obtained for APOD, PD and POD were at modulation index of 1.0 with values of 277.30V, 277.10V and 277.00V, while the lowest output voltage was obtained at modulation index of 0.2 with voltage values of 29.45V, 28.07V and 29.45V respectively. A minimal power loss of 0.92W was obtained in the entire carrier signal used. The finding of this work established that as modulation index increases, the THD of the CHB MLI decreases with the modulation index for APOD, PD and POD vary inversely with the THD generated by the carrier signals. The values of the output voltage, current and power increases with increase in modulation index while the PD carrier signal generates the lowest harmonic distortion at higher modulation index*

KEYWORDS*: Cascaded, multilevel inverter, SPWM, APOD, PD & POD, and THD*

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I. INTRODUCTION

The major drawbacks of conventional inverter are high cost, low efficiency and high switching loss [1], [2]. These drawbacks are the motivation behind developing multilevel inverter to mitigate these challenges. Multilevel Inverters are classified into three main types: Diode-clamped, Flying capacitor and Cascaded H-bridge multilevel inverters [3]. Cascaded H-bridge multilevel inverter have a modular structure and requires least number of components compared to diode-clamped and flying capacitor multilevel inverters [4]. This informed the choice of cascaded H-bridge multilevel inverter for the implementation of this work.

The conventional three-phase seven-level CHB MLI has thirty six switches and nine separate input DC sources [4]. The proposed asymmetric seven-level CHB MLI with reduced switches and DC power sources have eighteen switches and six separate DC sources which will reduce circuit cost and switching losses. In addition, it has the advantage of simple DC buses regulation, modularity of control and it requires least number of components to achieve the same number of voltage levels among compared to other multilevel converters [4], [5], [6].

II. ASYMMETRIC CASCADED H-BRIDGE MLI

This is the type of cascaded H-bridge multilevel inverter in which at least one of the DC supply source presents different amplitude, that is H-bridge cells are not fed by equal voltage and the arm cells have different effect on the output voltage steps [7].

The circuit diagram of three-phase seven-level asymmetric cascaded H-bridge multilevel inverter with reduced number of switches is shown in Figure 1.0.Each phase has two legs, and it carries three switches in each leg. The switches are named asS_1, S_2 and S_3 to S_{18} and are arranged in the first and second leg of each phase respectively.

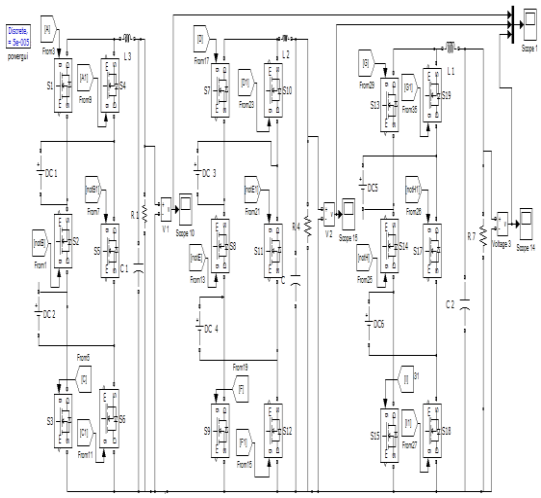

Figure 1: Circuit diagram of the 3-phase seven-level asymmetric cascaded H-bridge multilevel inverter with reduced number of switches

7-levels CHB MLI with reduced numberof switches.

For cascaded H-bridge multilevel inverter with N-level per phase, the output voltage per leg is the sum of all the individual inverter outputs.

The output voltage per leg is

$V_{an} = V_{a1} + V_{a2} + \ldots + V_{ax}(N-1)$ (1)

Where V_{an} = single phase output voltage

$V_{a1}, \ldots, V_{ax}$ = output voltage of individual inverter

N = number of voltage levels

And the phase voltage is expressed as

$V_{an}(\omega t) = \frac{4V_{dc}}{n\pi}[\sum_{j=1}^{n-1} \cos(m\alpha j)] \sin(n\omega t)$ (2)

where n = 1, 3, 5 ... (positive odd numbers)

Each H-bridge unit generates a staircase waveform by level-shifting it's positive and negative ends. The modulation index m_a is given by

$m_a = \frac{\pi V}{4dc}$ (3)

The asymmetric seven-level Cascaded H-bridge multilevel inverter has two DC sources and six power switches per phase and the magnitude of DC input voltage sources are $100V_{dc}$ and $200V_{dc}$ in each phase as shown in circuit diagram of three-phase seven-level asymmetrical cascaded H-bridge multilevel inverter. The output voltage can be positive voltage ($+V_{dc}$), Zero voltage ($0V_{dc}$) and Negative voltage ($-V_{dc}$). Hence the desired voltage levels for seven-level asymmetric cascaded H-bridge multilevel inverter are from $+3V_{dc}$ to $-3V_{dc}$. The switching table of the switching states of single phase asymmetrical 7-level CHB MLI is as shown on Table 1.0.

Table 1.0: Switching states of single phase asymmetrical 7-level CHB MLI

S/N	Switching sequences S_1	S_2	S_3	S_4	S_5	S_6	Voltage levels
1	0	1	0	1	0	1	+3Vdc
2	1	1	0	0	0	1	+2Vdc
3	0	1	1	1	0	0	+1Vdc
4	0	0	0	1	1	1	0Vdc
5	1	0	0	0	1	1	-1Vdc
6	0	0	1	1	1	0	-2Vdc
7	1	0	1	0	1	0	-3Vdc

NOTE: 1 is in **OFF** state**. 0** is in **ON** state

III Switching Loss

The switching loss is proportional to the switching frequency and hence it contributes significantly to the inverter total loss, especially for inverters applying SPWM. The switching power loss (P_{sw}) during one second in a switch is defined by the formula

$$P_{sw} = \sum \frac{1}{2} V_d I_o t \quad (4)$$

Where V_d = Voltage over the switch when the switch is OFF, I_O is Current through the switch when it is ON or before turn off and **t** is either turn on time or turn off time. The sum of all turns on and turns off during one second for one switch result is the switching power loss. The switching power loss can be defined by the equations:

$$\text{Turn on} = \frac{1}{2} V_d I_o t_{-on} \quad (5)$$

$$\text{Turn off} = \frac{1}{2} V_d I_o t_{-off} \quad (6)$$

Therefore the sum of the switching power losses is.

$$P_{sw} = \sum \left(\frac{1}{2} V_d I_o t_{on} + \frac{1}{2} V_d I_o t_{off}\right) = N_{sw} \sum E_{sw.tot.} \quad (7)$$

Where N_{sw} = the number of switches in the inverter.

The power loss is calculated based on the value of modulation index chosen for any of the carrier signals. For APOD, at the modulation index of 1.0, switching loss will be:

$$P_{sw} = N_{sw} \sum (E_{sw-OFF} + E_{sw-ON}) \quad (8)$$

For V_d =277.30, I_o = 2.77, t = $2x10^{-4}$s and f = 5 kHz

P_{sw} (Both ON and OFF) = 0.153624W.

Similarly, the switching loss of PD and POD are approximately the same as APOD.

IV Filter Analysis

Low pass LC filter with resistive load is chosen for the implementation of this work. A single inductor was connected in parallel with a single capacitor. Input signal (V_{in}) is applied to the parallel combination of the inductor and the capacitor but the output signal (V_{out}) is taken across the resistive load only. The cut-off frequency is 50Hz. The filter equation will be:

$$f_c = \frac{1}{2\pi} \frac{1}{\sqrt{(LC)}} \quad (9)$$

For f = 50Hz, C = 6800µF and R = 100Ω, then L= 1.49mH

V SINUSOIDAL PULSE WIDTH MODULATION CONTROL CIRCUIT

Figures 2.0 shows the modulation control logic circuit for the carrier signals. These control circuit generates pulses that control the switching pattern of the MOSFET switches in the H-bridges. And this is based on the type of carrier disposition that will be chosen for the implementation in the research work.

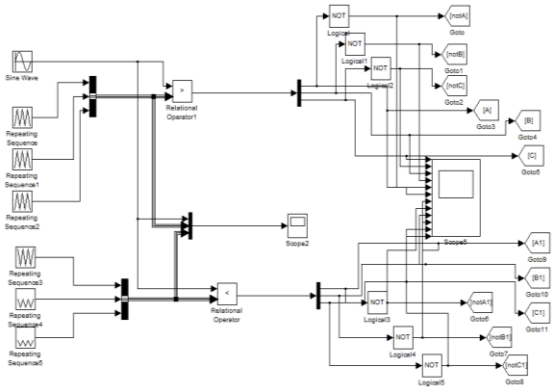

Figure 2.0: modulation control circuit using POD carriers signal

Different control techniques exert different effects on different topologies of MLI. Some affect harmonics, others the voltage levels while others the output power [8], [9] and [10]. The choice of the modulation strategy to be developed for a particular family of converters is predicated upon switching frequency, distortion level, harmonic generation, speed of response and losses.

In sinusoidal pulse width modulation (SPWM) technique, the signal is generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c [11]. The frequency of the reference signal determines the output frequency and its peak amplitude that controls the modulation index M_a. In this presents work, sinusoidal PWM is used because it has high switching frequency and reduction in the total harmonic distortion and switching losses [12], [13].

The number of carrier waveforms m needed to produce N voltage level output is

$$m = N - 1 \quad (10)$$

The single sinusoidal reference waveform has peak to peak amplitude of A_m and a frequency F_m. The multiple triangular carrier waves have same peak to peak amplitude and frequency F_c. The frequency ratio M_f is as follows.

$$M_f = \frac{F_c}{F_m} \quad (11)$$

The amplitude modulation index for the carrier signal is

$$M_a = \frac{A_m}{A_c} \quad (12)$$

The **c**arrier signals used in this work are PD (Phase Disposition), POD (Phase Opposition and Disposition) and APOD (Alternate Phase Opposition and Disposition).

VI RESULTS AND DISCUSSION

MATLAB/SIMULINK was used to simulate the asymmetric MLI for an APOD carrier signal using modulation index from 0.2 to 1.0 and the results are as presented in Figures 3.0 to 8.0 and Table 3. At modulation index of 0.2, very high THD of 76.98 % was measured and very low output power of 8.67 W. At the highest modulation index of 1.0, the fundamental frequency measured from the scope was found to be 265.1Hz while the output voltage and power significantly increased to 277.3V and 768.95 W with corresponding THD of 22.22 % and current of 2.77A

It can be deducted that at lower modulation index, there is high THD and high power loss while high modulation index, there is low THD and less power loss.

Figure 3.0: Simulation output of triggering signals of 12 switching circuit of single phaseseven-level CHB MLI using APOD. which is equivalent to that of PD and POD

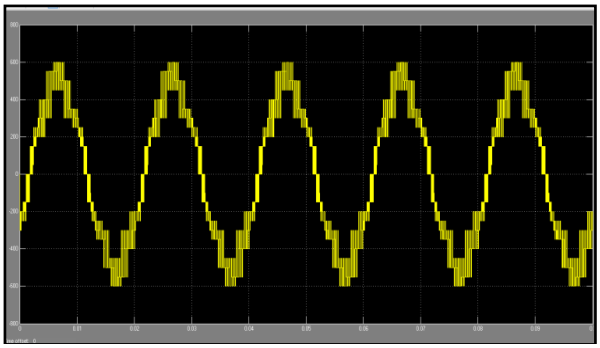

Figure 4.0: Line to line output voltage waveform of asymmetric seven-level single phase CHB MLI using APOD carrier signal. .which is equivalent to that of PD and POD

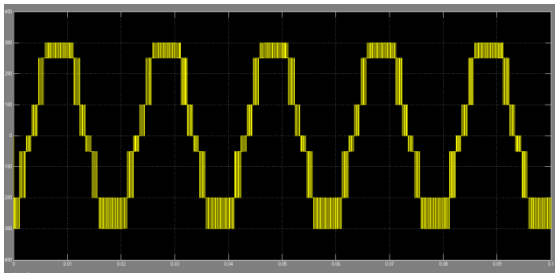

Figure 5.0: Lines to ground output voltage waveform of single-phase seven-level CHB MLI using APOD carrier signal. .which is equivalent to that of PD and POD

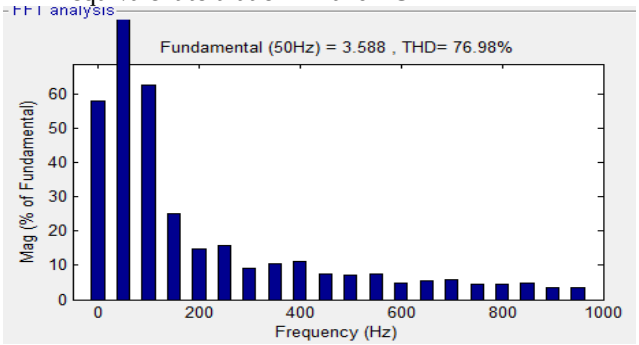

Figure 6.0: THD of APOD at m_a = 0.2 of single-phase Seven-level CHB MLI

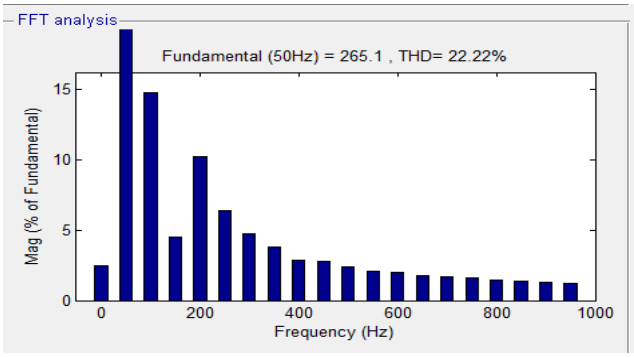

Figure 7.0: THD of APOD PWM at m_a = 1.0 of single-phase seven-level Cascaded H-bridge multilevel inverter

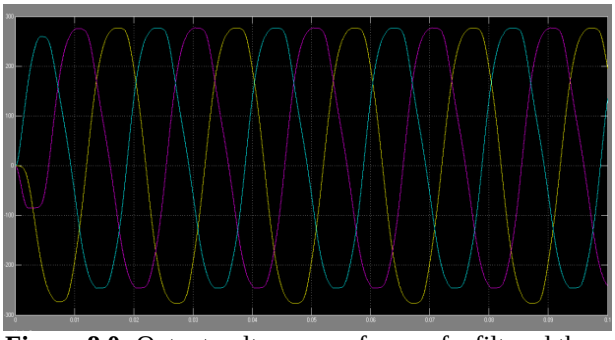

Figure 8.0: Output voltage waveforms of a filtered three-phase seven-level Asymmetric CHB MLI using APOD carrier signal .which is equivalent to that of PD and POD

Table 2: THD, Output voltages, Output current and Output power of single-Phase Seven-level CHB MLI using APOD carrier signal.

s/n	M_a	THD %	Output Voltage (V)	Output Current (A)	Output Power (W)
1	0.2	76.98	29.45	0.29	8.67
2	0.3	72.08	39.41	0.39	15.53
3	0.4	75.28	99.70	1.00	99.40
4	0.5	63.75	102.90	1.03	105.88
5	0.6	44.33	181.30	1.81	328.70
6	0.7	36.49	222.30	2.22	494.17
7	0.8	31.99	239.10	2.39	571.69
8	0.9	24.48	268.70	2.69	722.00
9	1.0	22.22	277.30	2.77	768.95

Results using PD carrier signal with varying values of modulation index from 0.2 to 1.0 are as presented in Table 3. At the peak modulation index of 1.0, the fundamental frequency measured by the scope is 264Hz and the power qualities measurements at this value turn out to be maximum values. The maximum output voltage, THD, output power and current are 277.1V, 22.10%, 767.84W and 2.77A respectively.
The worst power quality values were at modulation index of 0.2. The least values of the THD, output voltage, current and output power are 79.58%, 28.07V, 0.28A and 7.88W respectively.

Table 3: THD, Output Voltages, Output Current and Output Power of Single Phase Seven-Level CHB MLI using PD Carrier Signal.

s/n	M_a	THD %	Output Voltage (V)	Output Current (A)	Output Power (W)
1	0.2	79.58	28.07	0.28	7.88
2	0.3	74.74	38.21	0.38	14.60
3	0.4	73.70	100.00	1.00	100.00
4	0.5	63.72	103.30	1.03	106.71
5	0.6	44.29	181.40	1.81	329.06
6	0.7	36.16	223.60	2.24	499.97
7	0.8	31.92	238.90	2.39	570.73
8	0.9	24.20	268.60	2.69	721.46
9	1.0	22.10	277.10	2.77	767.84

The results obtained from POD carrier signal are presented on Table 4. At the highest modulation index of 1.0 the fundamental frequency measured from the scope was 263.6Hz; the output voltage peaked at 277.0V with the least THD of 22.09%. The maximum output power of 767.29W and output current of 2.77A were obtained the same modulation index.

At the lowest modulation index of 0.2, the THD was 76.98% and the output power was 8.67 W. This is the worst power output as shown on Table 5. The output power keeps increasing as the modulation index increases.

Table 4: THD, Output voltages, Output Current and Output Power of Single Phase Seven-Level CHB MLI using POD Carrier Signal

S/n	M_a	THD%	Output Voltage(V)	Output Current(A)	Output Power(W)
1	0.2	76.98	29.45	0.29	8.67
2	0.3	72.08	39.40	0.39	15.52
3	0.4	74.57	100.10	1.00	100.10
4	0.5	63.19	103.10	1.03	106.30
5	0.6	44.47	181.70	1.82	330.15
6	0.7	36.39	223.70	2.24	500.42
7	0.8	32.14	238.90	2.39	570.73
8	0.9	24.32	268.80	2.69	722.53
9	1.0	22.09	277.00	2.77	767.29

VII CONCLUSION

This work has been able to establish that as modulation indexincreases, the THD of the asymmetric seven-level CHB MLI decreases regardless of the modulation technique adopted in the gating control signal technique. Therefore, the modulation index for APOD, PD and POD sinusoidal pulse width modulation (SPWM) vary inversely with the THD generated by these carrier signals. The values of the output voltage, current and power increases with increasing values of modulation index.

It is also worth noting that the POD carrier signal generates the lowest harmonic distortion at higher modulation index. The work therefore confirmed earlier assertion by a similar work of [10]

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